# Design and Performance Investigation of Compact and Fast Metaphotonics All-Optical Digital OR Gate

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***Abstract*—The paper presents an all-optical OR logic gate utilizing the phenomenon of light beam interference. The silicon substrate contains a two-dimensional photonic crystal (2D-PC) structure, which is created by arranging air holes in a precise configuration. A thorough investigation of the proposed metaphotonics gate is carried out using the finite-difference time-domain (FDTD) method. The findings highlight the gate's capacity to precisely execute its truth tables at a wavelength of 1550 nm, which is essential for C-band fiber-optic communication systems. The construction of the device has a unique bend geometry of 60 degrees, which results in a minimum device area of 40.8 $\mu$m$^2$, a high contrast ratio (CR) of 11.23 dB, and fast response time of 0.105 ps.**

***Index Terms*—2D-Photonic Crystal, Metaphotonics, Photon Interaction**

## I. Introduction

Since its invention, 2D-PCs have attracted attention as a means of enhancing optical-based systems because of their tiny size and capacity to manipulate light [1], [2]. A 2D-PC is a central component consisting of periodically arranged matrix of nano airholes within a silicon substrate [3]. By establishing a photonic band gap (PBG), this arrangement blocks the transmission of electromagnetic waves lying within the desired frequencies. Various studies have used the nonlinear Kerr effect to realize specific optical digital gates [4]. The associated limitations of high power consumption and complicated fabrication can be mitigated through interference-based defect approach. Optical waves interacting at the gate's combiner port can result in either constructive interference (logic '1') or destructive interference (logic '0'). The waveguides are created in the 2D-PC with line defect in a triangularly placed airhole matrix on silicon substrate shown in Fig. 1.

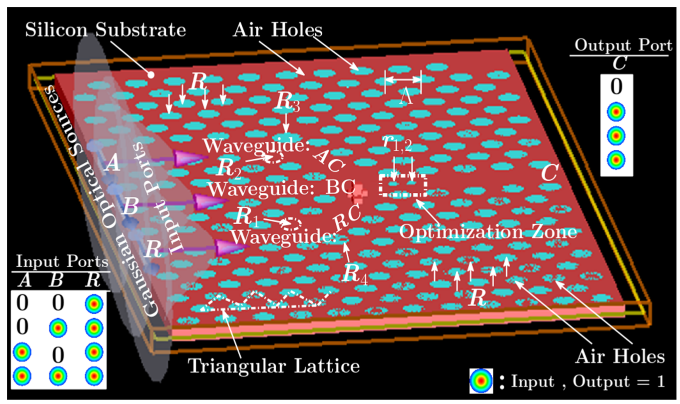


Fig. 1. Schematic of proposed OR gate with input (A & B), reference (R), and output (C) signal ports. The waveguide is optimized in 2D-PC by varying airhole and optimization zone radii, respectively.

## II. Device Optimization, Results, and Discussions

In the suggested concept, a silicon substrate with recurring circular air-holes is integrated into a triangular lattice array. The device now only measures 40.8 $\mu m^2$ with matrix airhole (including the missing holes at bends $(R_{1,2})$ radii of 124 nm, optimized airhole radii at bends $(R_{3,4})$ as 165 nm, lattice constant $\Lambda$ of 415 nm, and optimizing column airhole radii $(r_{1,2})$ of 58 nm, respectively. Furthermore, to enhance the waveguide's performance in terms of contrast ratio $[CR = 10 \log{(P_1/P_0)}]$, which measures the difference between logic '1's maximum output power and logic '0's minimum output power. The FDTD approach, which is renowned for its temporal efficiency, is applied in all ensuing simulations [5]. The edges of the structure are made up of perfectly matched layers, or PMLs. Gaussian optical input sources with specified power $P_{in}$ levels are connected to the input ports (*A*, *B*, and reference port *R*) of the gate. Output power exceeding 30% of the expected input power is categorized as logic '1', while output power falling below 30% is classified as logic '0'. The C-band (1535 nm to 1565 nm) has a source wavelength of 1550 nm, according to bandstructure calculations. The output powers for the digital input combinations have been shown in Fig. 2. Consequently, a CR of 11.23 dB and an average response time (RT) of 0.105 ps have been obtained.

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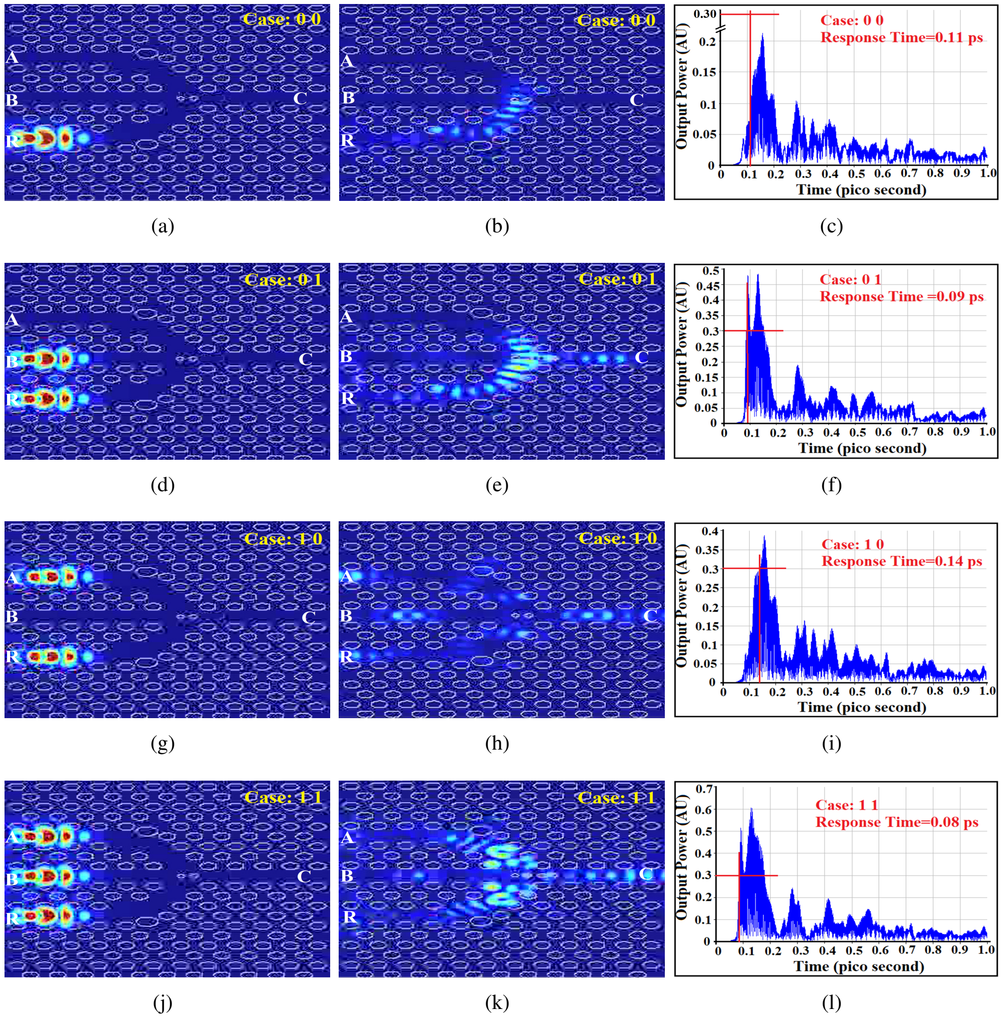


Fig. 2. Optical waves enter from the input and reference ports in waveguides *A, B, & R* and exit from the output port *C*. Here, **Case: 0 0** has been depicted by (a)-(c), **Case: 0 1** by (d)-(f), **Case: 1 0** by (g)-(i) and **Case: 1 1** by (i) and (l).

TABLE I
OPTIMUM PARAMETERS

| **Reference** | **Logic Gate** | **Area ($\mu$m$^2$)** | **CR** | **R (ps)** |
|---|---|---|---|---|
| [6], 2015 | AND-OR-XOR | 130 | 16.7-20.3 | 3 |
| [7], 2021 | AND & OR | 140.8 | 6.64 | 0.784 |
| This Work | OR | 40.8 | 11.23 | 0.105 |

An overview of the results is shown in Table I, where they are compared with other published studies on all-optical OR gates. The provided optical OR gate has the minimal device area of 40.8 $\mu$m$^2$.

## III. CONCLUSIONS

In this work, a metaphotonics all-optical OR logic gates has been developed. Numerical simulations verify that the proposed structure fulfills the truth table at 1550 nm with an OR gate contrast ratio of 11.23 dB, response time of 0.105 ps, and a minimum area of 40.8 $\mu$m$^2$. The optical chips that are intended for use in quantum communication can be made using the designed gate.

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