# Investigation of a Double-Intra-Cavity VCSEL at cryogenic temperatures

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*Abstract***— Vertical cavity surface-emitting lasers (VCSELs) operating at cryogenic temperatures are developed for energyefficient optical links due to their low power consumption and high bit rate, these devices require precise alignment of cavity resonance and peak gain at the target temperature. Understanding the junction temperature of the operating device is crucial for the design. We conducted a thermal and electrical analysis of a double-intra-cavity VCSEL specifically designed for operation at cryogenic temperatures.** 

## *Keywords—intra cavity, VCSEL, cryogenics, thermal modeling, low temperatures.*

# I. INTRODUCTION

The effort to reduce the size of CMOS technology to meet increasing computational demands has led to unsustainable power consumption in data centers, highlighting the necessity for alternative computational methods. Superconducting processors using single flux quantum (SFQ) technology have gained significant interest for their power efficiency, even when accounting for cooling requirements. Recently, there has been a growing need for efficient optical interconnects to enable highspeed data transfer from cryogenic environments to roomtemperature data storage [1]. High-speed, low-power verticalcavity surface-emitting lasers (VCSELs) capable of operating at cryogenic temperatures are seen as a promising solution [2- 4]. The VCSELs performance at cryogenic temperatures presents new challenges due to changes in physical parameters such as refractive index, thermal conductivity, mobility, bandgap, and activated dopants, necessitating new design strategies .

In this study, we present a thermal and electrical analysis of a double-intra-cavity (DIC) VCSEL operating over a wide range of temperatures. To reduce drive voltage and improve power conversion efficiency at cryogenic temperatures, a double intracavity contacted design is used. As depicted in Fig. 1, the wavelengths of the cavity resonance mode and the gain peak shift at different rates as the temperature changes. To address this, the VCSEL gain profile is intentionally detuned from the

cavity resonance at 300 K, ensuring that the gain peak aligns with the cavity resonance at cryogenic temperatures. Since the values of the cavity resonance and the gain peak are temperature-sensitive, knowing the actual temperature of the operating device is crucial for better design.



Fig. 1. Variation of Fabry–Pérot (FP) dip and peak gain with temperature. The  $T=50K$  is the lowest temperature achieved by the Harold® (by Photon Design).

## II. THERMAL ANALYSIS

When the VCSEL is operational under lasing mode, various power dissipation mechanisms, such as non-radiative recombination, Joule heating, free-carrier absorption (FCA), scattered stimulated emission, and spontaneous emission not coupled into the lasing mode, contribute to heating the device. Among these, FCA and Joule heating are particularly significant in heating the active area. The experimental results of series resistance and the corresponding Joule heating of an operating but non-lasing DIC-VCSEL at two different temperatures are depicted in Fig. 2. Since the doping levels in the p-and n- contact layers are above the Mott criterion ( $\approx$  4e + 18 for p-GaAs and  $\approx$  2e + 18 for n-GaAs) [5], we can assume that most of the carriers are fully ionized even at very low temperatures. Therefore the FCA slightly changes ( $\approx$  from 0.8mW at 273K to

0.92mW at 47K at 10mA, extracted from Harold® by Photon Design) as the temperature decreases.



Fig. 2. Measured differential resistance of a DIC-VCSEL at two different temperatures.

By extrapolating the Joule heating for a drive current of 10mA, using the thermal conductivity of  $Al_xGa_{1-x}As$  [6], and utilizing a thermal simulation using finite-element method in COMSOL Multiphysics®, the rise in temperature of the active area can be seen in Fig. 3 (a) and (b).



Fig. 3. (a). A schematic picture of an operating 4μm-aperture DIC-VCSEL that is thermally insulated from the top side and thermal radiation is considered from metal pads and contacted to the cryogenic plate from the bottom of substrate. The DIC-VCSEL structure consist of 1λ thick cavity with three In<sub>0.12</sub>Ga<sub>0.88</sub>As 5nm quantum wells surrounded by 5nm  $Al_{0.12}Ga_{0.88}As$  barrier layers. Undoped GaAs (59.2nm)/AlGaAs (71.4nm) top and bottom DBRs consist of 21 and 30 periodes respectively formed the laser cavity structure. Pcontact and n-contact layers are 572nm of 4.5e+18 Be-doped and 490nm Sidoped GaAs respectively. The oxidized DBR layer to form the oxide layer consists of  $21nm/ Al_{0.12}Ga_{0.88}As, 14.5nm/ Al_{0.9}Ga_{0.1}As, 30nm/ Al_{0.98}Ga_{0.02}As,$ 14.5nm/  $Al<sub>0.9</sub>Ga<sub>0.1</sub>As, and 21nm/ Al<sub>0.12</sub>Ga<sub>0.88</sub>As. (b) Colored lines indicate the$ thermal conductivity of  $Al_xGa_{1-x}As$  with different Al percentage at different temperatures. The temperature of an operating DIC-VCSEL increases to higher values as depicted with the balck line.

#### III. ELECTRICAL ANALYSIS

In this section, using the information obtained from the thermal analysis, an electrical analysis is performed. The structure is designed to operate at a temperature of 4 K. However, The temperature-dependent L-I-V (light-currentvoltage) curves of the cryo-DIC VCSEL are illustrated in Fig. 4 down to 50K. The increase in voltage may result from increased potential barriers at heterojunctions within the cavity.



Fig. 4. Output power and the voltage of the cryo-DIC VCSEL versus current at different temperatures. As can be seen, the threshold current decreases as the temperature decreases because the FP dip and the peak gain align at low temperatures.

### IV. CONCLUSION

To design the cryogenic DIC-VCSEL more accurately, knowing the actual operating temperature of the device is crucial. To determine the device temperature, a thermal analysis was performed. The electrical analysis showed that with a precise design, the peak gain and the cavity resonance aligned at 50 K, resulting in a reduced threshold current. Future design effort will aim to minimize DIC-VCSEL power consumption at cryogenic temperature close to 4K.

# ACKNOWLEDGMENT

Authors wish to acknowledge funding from EU under grant agreement 899558 towards project aCryComm and in part by microwave metrology for Superconducting Quantum circuits (SuperQuant) under grant agreement 20FUN07 and in part by Academy of Finland flagship program PREIN (decision 320168).

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