Photonic Integrated Circuit Design Flow in 45 nm SOI GF Fotonix™ Platform

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***Abstract*—Design and simulation flow for different photonic devices and circuits are discussed in this paper. Two different circuit design flows, namely Cadence Virtuoso based and Ansys Lumerical based flows are used to study an add-drop micro-ring resonator device and, 4x4 switch circuit using GF Fotonix™ PDK. The simulation results are exhibiting close match with the hardware data obtained from the GF 45 nm SOI process technology.**

***Index Terms*—Design flow, simulation flow, switch matrix, micro-ring resonator, 45 nm SOI**

I. Introduction

With rapid progress in silicon photonic research and development over the past decade, there has also been a parallel growth in multiple tools and reference flows for design and simulation of the photonic devices, circuits and systems. Hence, alternate simulators are very impactful in verifying a circuit's working while the industry is still in progress of standardizing the design flow for integrated photonics. As a major silicon photonics foundry offering MPWs to customers, it is important to ensure that the GlobalFoundries PDK can support multiple EDA tools and cater to custom design flows.

In this paper, we discuss two different simulation flows. One of the flows highlights the Cadence Virtuoso flow and the other shows the Ansys Lumerical flow. To validate the design flows, a micro-ring resonator (MRR) in add-drop configuration [1] and a Mach-Zehnder interferometer (MZI) based switch circuit have been implemented as two test cases for a device and a circuit respectively. The simulation data from both the flows have been verified with measured hardware data.

II. Circuit Design Flow

Two different flows for simulating the photonic circuits using GF PDK is presented in this section. First, the Cadence Virtuoso simulation is discussed using the GF PDK based photonic device compact models. In the Ansys Lumerical flow, mainly the following steps are required. First, the passive device simulations are performed using Lumerical MODE, FDTD or EME solvers. Few specific device parameters such as an MRR radius or coupling co-efficient can also be directly used as per the PDK specification in the Interconnect component model without performing the device simulation. Different circuit simulation results like passive transmission, transient response, eye diagram, etc can be obtained from INTERCONNECT.

III. Results and Discussion

In this section we will discuss about a device simulation and a circuit simulation using the aforementioned steps. We are demonstrating an add-drop microring resonator and a Mach-Zehnder based 4x4 switch. The simulation as well as the hardware data is shown for both the cases.

A. Add-drop microring resonator

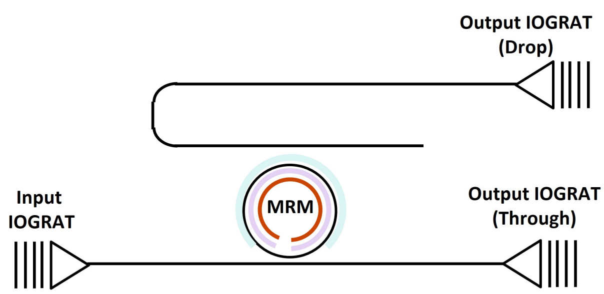

Fig. 1. Schematic diagram of a micro-ring resonator in add-drop configuration.

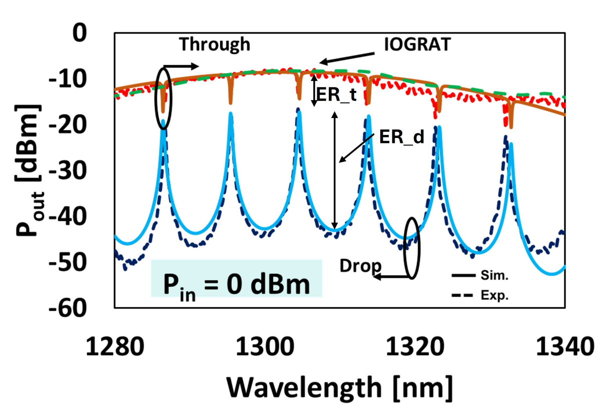

Fig. 2. Transmission characteristics of an add-drop microring resonator for 0 dBm of input power. Solid lines show simulation data from compact model and dotted lines is measured data.

Fig. 1 shows a schematic of an add-drop micro-ring resonator. It has a radius of 7.5 μm, with 240 nm gap between the ring and both the bus waveguides. This device exhibits a free spectral range (FSR) of ~9.2 nm with Q-value of 5000±500. The through port extinction (ER_t) is ~6 dB and the drop port exhibits (ER_d) ~25 dB as shown in Fig.2. The variation in extinction is ±1 dB across 12 sites in 3 wafers. Fig. 2 also shows the measured as well as simulated response from Cadence Virtuoso for the add-drop micro-ring resonator for an optical power of 0 dBm at the input grating coupler. The grating couplers have insertion loss of ~ 4.2 dB each.

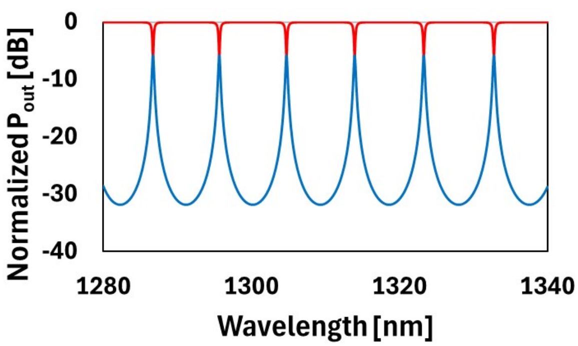

Fig. 3. Normalized transmission characteristics of an add-drop microring resonator obtained from Ansys Interconnect simulation.

Fig. 3 shows the response of the MRR of the same parameters without having the input-output grating couplers. Hence we observe similar values of FSR, Q value, and extinction but with the maximum output power of ~0 dB.

B. 4x4 switch matrix

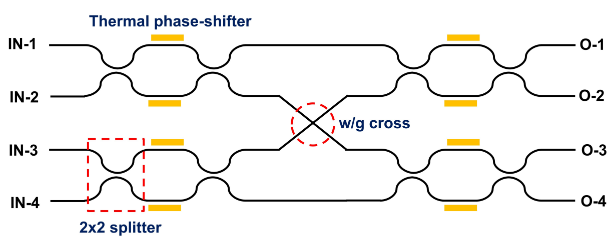

Fig. 4. Schematic diagram of a 4x4 switch.

To establish the flow for circuits, we are presenting a Mach-Zehnder based 4x4 switch as shown in Fig. 4 whose details can be found elsewhere [2]. Fig. 5 shows the output from port-1 when the input is at port-1. It shows that the other ports' output are less by ~20 dB. The measured data matches quite well with Cadence Virtuoso simulation data. The couplers/ splitters, waveguide crossings, tapers, waveguides were also simulated in Ansys MODE/FDTD/EME and fed into Interconnect. The simulated data from Ansys is shown in Fig. 6 which does not have the input-output grating couplers. The performance comparison of the important parameters for the 4x4 switch circuit is tabulated in Table I. The insertion loss (IL) and the crosstalk for channel-1 are within ±0.1 dB and ±1.5 dB for both the simulation flow and hardware respectively.

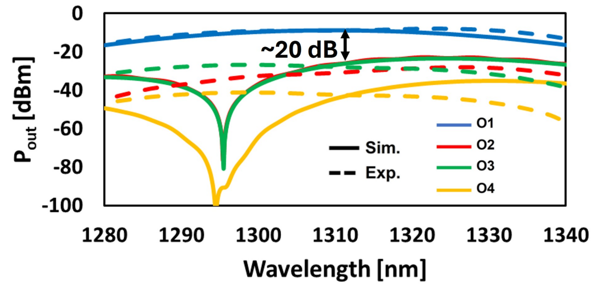

Fig. 5. Transmission characteristics of 4x4 switch from input-1 to output-1. Dashed lines are measured data, solid lines show simulation data.

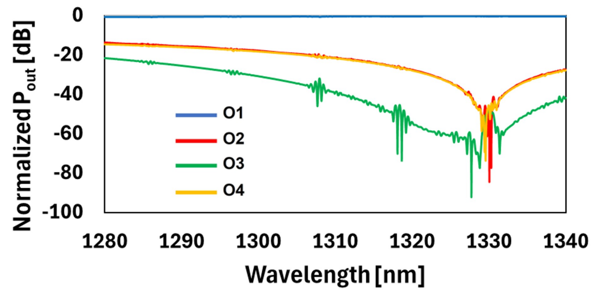

Fig. 6. Normalized transmission characteristics of the 4x4 switch from input-1 to output-1, obtained from Ansys Interconnect simulation.

TABLE I
SIMULATED VS. MEASURED VS. INTERCONNECT DATA FOR 4X4 SWITCH CIRCUIT

Parameteres @ 1310 nm	Compact Model	Experiment	Interconnect
IL(dB) (w/o IOGRAT)	0.6	0.6	0.41
Crosstalk(dB) for channel-1	17.7	18.9	21.1

IV. CONCLUSION

In this work we presented a comparative study of two design and simulation methods for photonics devices and circuits. The results from Cadence Virtuoso and Ansys Lumerical based flows for a microring resonator and a 4x4 switch circuit have been verified with hardware data using GF 45-nm SOI Fotonix^{TM} technology.

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