Efficient design and fabrication of CMOS Active Pixel Sensors through modeling and simulation

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Design and optimization of backside-thinned CMOS active pixel sensors (APS) using modeling and simulation is presented. For the efficient design and the further improvement of our backside-thinned CMOS imagers, different models were developed and TCAD simulating tools were used. The imagers have been successfully designed, fabricated and tested and proved to possess excellent imaging properties. This short abstract paper presents a summary of the models and simulations covering two critical design and processing issues, namely the epilayer (EPI) structure and the pixel isolating trench formation process as well as their influence on the electrical inter-pixel crosstalk.

I. Introduction

Since the past few years, the technology of complementary metal oxide semiconductor (CMOS) image sensor is taking the place of charged coupled device's (CCD) technology in many applications. One of those being the space investigation, the developed imagers should exhibit very high quality properties in terms of low electrical crosstalk. To be comparable with CCDs high quantum efficiency is also a prerequisite. In order to design and manufacture CMOS active pixel sensors (APS) with excellent imaging properties, different TCAD software tools can be used. For the design of our CMOS APS we used the combination of a Process and a Device simulator.

Among the other benefits of using a Process simulator, it was of great importance because it makes easier the evaluation and optimization of novel processing technologies such as graded EPI and deep trench isolation. Both those technologies are implemented in our CMOS APS devices. On the other hand, with a Device simulator, the electrical, thermal and optical characteristics of the device can be predicted. Thus, by combining multiple pixels in the same model, the inter-pixel electrical crosstalk was investigated.

II. Simulations

In the present model a five pixel array structure is taken into consideration. The purpose of the simulations is to see the crosstalk as a function of the doping profile and of the presence of trenches. The thinned backside illuminated detectors that are modeled have (a) a constant (Fig. 1) and (b) a continuous gradient doping profile (Fig. 2). The graded doping profile produces a built in electric field which guides the minority carrier flow. This acts in a synergetic way, helping to control the carrier diffusion mechanism.

Additionally, a structure incorporating trenches is developed (Fig. 3). Parameters of the models can be structural ones (thickness of the substrate, dopants profile and concentration,

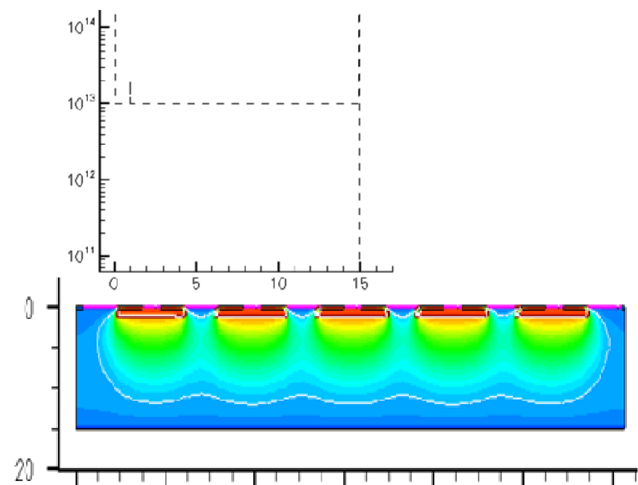

Fig. 1: Overlapping of depletion regions with the constant concentration EPI substrate

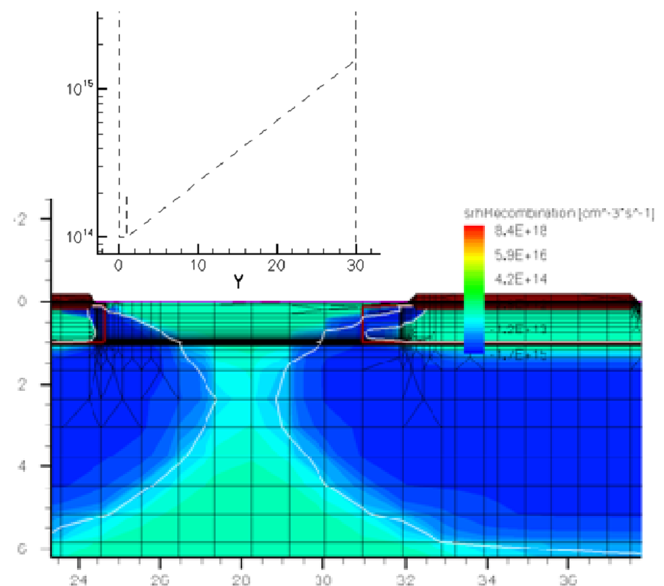

Fig. 2: Graded EPI parameters optimization

thickness of trenches, damage at the edges) as well as operating ones (wavelength/intensity of the illumination, applied voltage to the center and/or the neighboring pixels). Ray trace model is used for simulation of light interaction with the thin backside illuminated detector. It should be noted that light is coming from bottom of the structure (back-side illuminated APS).

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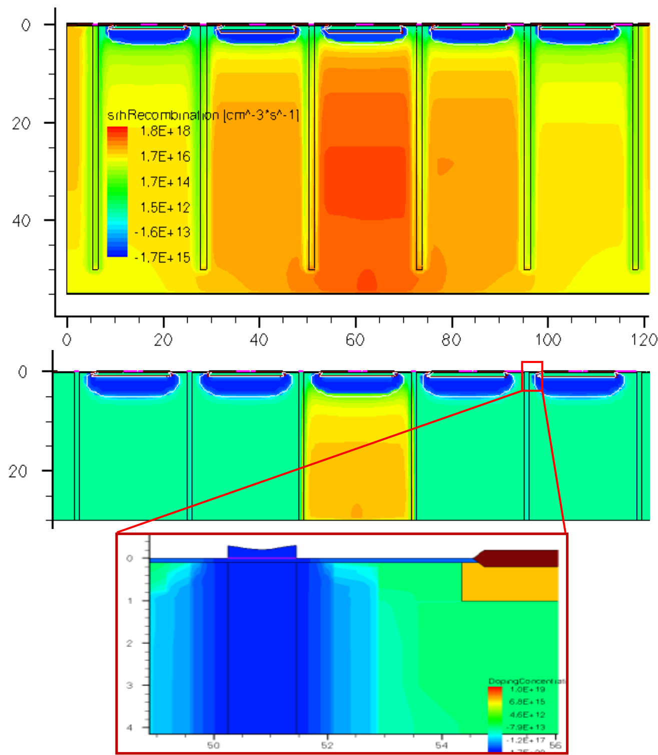

Fig. 3: Evaluation of the crosstalk for a thick (50um) and a thinner (30um) structure with pixel separating trenches (use of the process simulator to simulate the etching and polySi filing of trenches)

By implementing the model in the Sentaurus TCAD tool, the dopant profile and concentration for the desired substrate thickness was optimized (thickness is decided also by QE considerations). Then, it is possible to investigate further options, e.g. backside biasing. In Fig.1 and Fig.2 the simulated results in the case of biasing all the pixels at 1.6V, for two different sets of parameters concerning the EPI layer are presented.

As it can be seen, for the first case, where the substrate dopant concentration is too low (compared to the second case) and the bias voltage is too high, depletion regions are overlapping. This results in charge redistribution across pixels increasing the crosstalk.

For the case of the trenched imagers, the simulated results of the crosstalk, modeled using the Shockley-Read-Hall recombination are depicted in Fig.3. The trenches, incorporated into the model using the Process Simulator, are represented by regions of highly doped polySi. The formation of the trenches (e.g etching and filling) and the processing parameters are included in the model. In the inset is presented the detail of a trench, modeled following the same processing steps as in reality. The simulated crosstalk value was in the order of 5×10^{-4}.

III. Experiment

Using the conclusions from various simulations, thinned backside illuminated CMOS imagers were developed, combining a 30 µm EPI layer with varying doping concentration and trenches to reduce crosstalk [1]. The picture

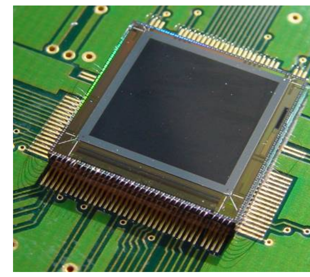

Fig. 4: Picture of completed 512x512sensor mounted on a PCB

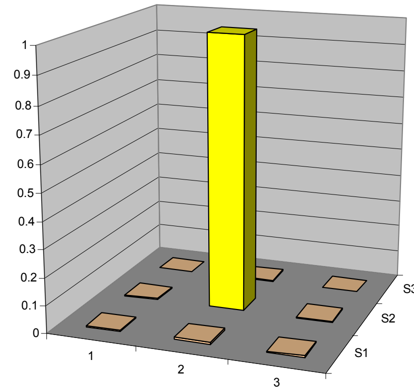

Fig. 5: Measured cross-talk of the trenched 1kx1k imager normalized to the center pixel signal

of a completed sensor assembly is shown in Fig.4.

Accurate characterization of crosstalk was performed using single spot illumination technique. In this case, a HeNe laser source providing a laser spot smaller than the pixel was used to stimulate a single pixel of the detector Fig. 5 presents the Point Spread Function (PSF) of a trenched device. A first measure of crosstalk is given by the ratio of the output signal of the neighboring pixels to that of the center pixel. As it is clearly depicted, all the incident signal is collected from the central pixel. Quantitative measurements from the specific pixel give a maximum crosstalk value of 8.2×10^{-3}, which is in the noise level and well below the specifications. The measured results show the efficiency of the modeling in the design phase of our CMOS imagers.

IV. Conclusions

We have presented the use of TCAD simulation software in the design of CMOS APS and the link between theoretical design and practical realization of a device. The backside-thinned CMOS imagers that have been successfully designed, fabricated and tested, possess excellent electrical inter-pixel crosstalk, as predicted by the simulations. Using the same tools or different analytical models, various sophisticated design issues such as radiation tolerance, antireflective coating and optimization of quantum efficiency are also investigated. An overview of those results will be presented in the full paper.

References

[1] K. De Munck, K. Minoglou, R. Padmakumar, D.S. Tezcan, J. Bogaerts, I.F. Veltroni, C. Van Hoof, and P. De Moor, "Monolithic and Hybrid Backside Illuminated Active Pixel Sensor Arrays," Proceedings of SPIE, vol. 7474, 2009, pp. 74741B-74741B-10.