PSPICE Models for Dye Solar Cells and Modules

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***Abstract*– A Circuital model for Dye Sensitized Solar Cell is proposed. Experimental comparisons and module design are carried out with the present model.**

INTRODUCTION

Dye Solar Cells (DSCs) are a promising low cost PV technology [1,2]. The choice of cell geometry and interconnection strategy is a crucial issue to design high performance devices [3, 4].
Efficiency losses due to substrate resistances and reduction of active area due to electrical contacts and device sealing are determinant aspects to consider in module design [3].
Here we show a simple and powerful DSC modelling carried out by PSPICE tool. The most diffused interconnection schemes were considered: Z, W and Parallel [5].
Z type modules utilize a vertical conductor to interconnect photoelectrode and counterelectrode of neighbouring cells. Differently from the Z, the W type modules avoids vertical interconnects by juxtaposing cells facing in one direction with cells facing the opposite direction. The lack of vertical interconnects enables a smaller interdistance between cells, although current mismatch arises since half of the cells are illuminated from the counterelectrode and the rest from the photoelectrode. Finally in parallel modules, a current collecting grid is required in order to mitigate losses due to TCO sheet resistance.

THEORY

The circuit of the single cell is implemented by a GVALUE block. A GVALUE block in PSPICE allows to define a J-V characteristic only by including a given expression (i.e. the diode equation of the current).
For DSC Current-voltage behaviour we used the Butler-Volmer expression (1) described in [6].

$$J_{BV} = J_0\left(\exp\left(\beta \frac{e_0}{K_B T} V\right) - \exp\left(-(1-\beta)\frac{e_0}{K_B T} V\right)\right) \qquad (1)$$

The GVALUE Block is in parallel to a current generator that simulates the photocurrent produced. The Current generator and the GVALUE Block are connected in parallel to a resistance R_P of 2 kΩcm^2 and in series to R_{TCO} (resistance related to the Transparent Conductive Oxide), calculated using

$$R_{TCO} = \frac{R_{SH}\cdot(L+d)}{H} \quad , \qquad (2)$$

where R_{SH} is the TCO sheet resistance and (L + d) an H are the linear dimension of the cell as shown in Fig. 1 [4, 7].
We observe that R_{SH} is not negligible (~10 Ohm/sq) since to guarantee an high substrate transparency, TCO coating as thin as few hundreds of nm are required.

MODELLING FOR DSC MODULE

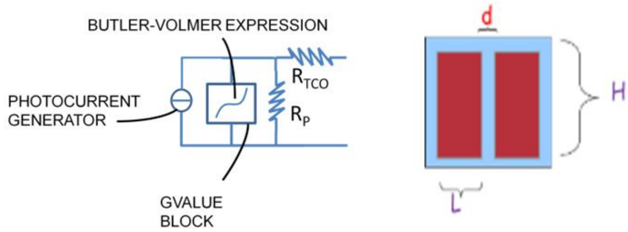
Different circuit models have been designed for Z /W series and parallel DSC modules.
The equivalent circuit of a single cell furnishes electrical J- V characteristics that are in well agreement to experimental results. Each cell is then connected in series or in parallel according to the module electrical scheme.
For parallel scheme, the whole series resistance of the cell is modeled by the series of two resistances (Fig. 2a): R_{finger} and R_{TCO}. R_{finger} simulate the losses due to the current path length and can be expressed according to the Ohm law as in

$$R_{finger} = \frac{\rho\cdot L}{t\cdot W} \quad , \qquad (3)$$

where *W* is the width, *H* the length, *t* the thickness of the grid and *ρ* the resistivity of the grid material.
R_P simulate the resistance of TCO of the cell in the parallel scheme, and is calculated as

$$R_P = \frac{R_{SH}\cdot L}{4H} \,. \qquad (4)$$

For Z type (Fig. 2a), R_{cv} represents the resistance of the vertical contacts between two cells and can be varied modifying the physical dimensions or the material resistivity.
For W module (Fig. 2b), two different cell blocks represent the front and the back illuminated cells. The width of the cell is balanced in order to have the minimum current mismatch.



a) b)

Fig. 1 :PSPICE circuit of Dye Sensitized Solar Cell (a) and typical layout of DSC Module (b).

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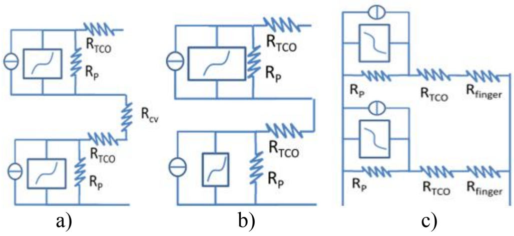

Fig.2: Circuit model for Z (a), W (b) and parallel (c) DSC modules.

RESULTS AND SIMULATIONS

We simulated Z, W and Parallel modules and compared the results with experimental I-V characteristics. Simulations show the level of reliability of the model considered.

Simulated and experimental data relative to parallel module are reported in Fig. 3 and in Table I, showing an evident accordance. Similar correspondence was found for others configuration.

To achieve the optimal DSC Z module geometry, we fixed the area of the module and varied the width (and the consequently also the number) of the cells. Each curve of Fig. 4, represent the power generated at maximum power point from each module configuration at different level of Jsc. The curves shows that the power generated by modules, with constant module area, is strongly affected by cell geometry. The most efficient geometry can be choose also considering the expected current density of the cells (i.e. depending on the features of the cell, as the used dye, the titania thickness, etc.). Table II evinces optimal geometry for three level of density current and the percentage lost with the not optimized Width of cell. This result indicates also the different optimal configuration with respect to a different illumination condition (Jsc is proportional to the power of illumination).

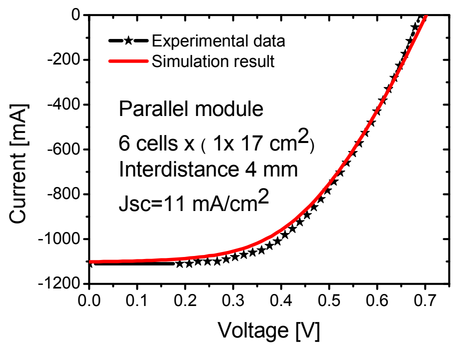

Fig. 3: Comparison between SPICE simulation and experimental data for Parallel DSC modules.

TABLE I
EXPERIMENTAL AND SIMULATED PARALLEL MODULE VALUES

Parallel module	Experiment	Simulation
Pmax [W]	0,405	0.392
Isc [A]	1.1	1.1
Voc [V]	0.69	0.7
Imax [A]	0.924	0.892
Vmax [V]	0.44	0.44
FF	53.3%	50.5%
Efficiency	3.7%	3.7%

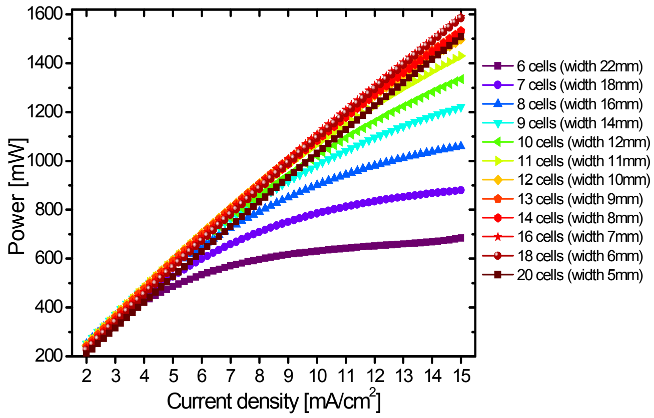

Fig. 4: result of several SPICE simulations of Z type DSC module on A5, (15x20) cm^2, substrate. The difference between the curves is the width and the number of the cells (length is fixed on 192mm).

TABLE II
LOST POWER COMPARED TO BEST TOPOLOGY (%)

# of cells	Jsc 6 mA/cm^2	Jsc 10 mA/cm^2	Jsc 15 mA/cm^2
6	-24.19	-43.17	-57.02
8	-7.67	-18.85	-33.31
10	-3.92	-8.07	-16.05
12	---	-1.28	-5.86
14	-3.58	-2.39	-3.7
16	-2.2	---	---
18	-4.55	-1.55	-0.38
20	-10.69	-7.15	-5.11

CONCLUSIONS

The model of DSC and DSC modules, for Z, W and parallel designs, has been validated by the comparison between simulation and experimental data. The simulation models implemented is confirm to be a valid instrument in order to design different schemes for large area DSC. Optimized layout considering resistance loss and active area lost were proposed at different Jsc and performance device.

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