Hybrid Electronic-Photonic Integrated Circuits: Hybrid FET-LET SRAM

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Abstract - **High speed, low power, low leakage, and low noise circuits are extremely essential for modern VLSI chips. Since on-chip cache memories consume appreciable amount of the total chip area and energy, high performance and low power Static Random-Access Memories (SRAMs) are needed for high performance and low power electronic systems. A hybrid FET-LET 6T SRAM, with the access transistors being replaced by Light Effect Transistors (LETs), has been proposed and analytically analyzed. Numerical analyses reveal that a prototype hybrid SRAM array of size 512KB show a factor of 18 and 17 reduction in read delay and read energy, respectively; and 2 and 4 reduction in write delay and write energy, respectively, compared to the conventional 6T SRAMs.**

***Index Terms*— SRAM, LET, access devices, low power, low leakage**

While photonic integrated circuits (PIC) are playing ever-greater roles in our technology ecosystem, the anticipated explosive growth has not yet happened, because of a few fundamental or practical challenges:[1] (1) size mismatch, because photonic devices are fundamentally limited by light wavelengths; (2) high energy-data rate (EDR), due to the energy efficiency of photonic devices when used for transmitting information in terms of joule per bit of the information transmitted;(3) cascadability and fan-out,[2] because of the inefficient conversion between optical and electrical energies. Therefore, in a current PIC, photonic components are typically used for interconnection between electronic sub-systems. Here we propose a novel approach that can overcome these limitations and thus allow photonic devices playing more active roles in information processing.

SRAMs are generally used in high speed caches providing a direct interface with the CPU at high speeds, and on chip caches typically consume a major portion of the total energy of a chip.[3] However, further improvement potential is limited to meet the ever increasing demands in speed and energy consumption within the conventional framework. Although photo-conductive devices like a Light Effect Transistor (LET),[4,5] may potentially offer advantages in switching speed and energy and even perform logic operations, they also face the cascadability issue.[6] To take the advantages of both LETs and FETs but avoid their shortcomings, we propose a hybrid FET-LET 6T SRAM that can offer major improvement on the overall performance by replacing the two access FETs with two LETs and the word line electrical wires with optical waveguides (OWGs). This application also avoids the well-known energy-data rate (EDR) challenge (EDR ≤ 10fJ/bit for on-chip communication),[7] since it is not required to use light to address photonic devices individually,[6] but in a group simultaneously through an OWG.

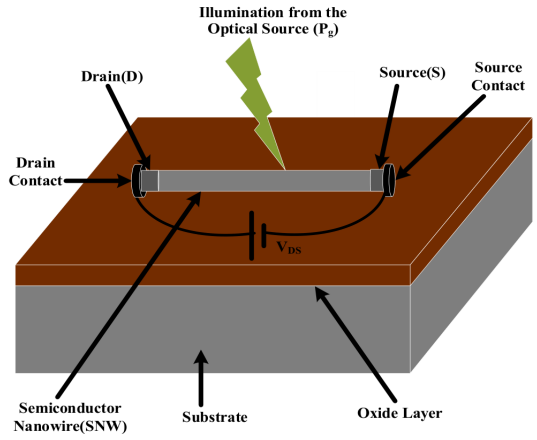

Fig. 1: Schematic of a Light Effect Transistor (LET)

A LET, as shown in Fig. 1, is a very simple structure with a semiconductor nanowire (SNW) placed on an insulating substrate with two metal contacts at the ends.[4] In the LET, the source drain conductivity is modulated by light of suitable wavelength as in a photoconductive device but with specific I-V characteristics.[4,8] The advantage of LET over a FET is due to the removal of physical gate, thus minimizing the complex gate fabrication process and random dopant fluctuations and gate related short channel effects (SCEs) which are common in nano-scale FETs. Since the LET does not have a physical gate, the device speed is expected to be only limited by the carrier transit time or lifetime, which-ever is smaller, rather than the capacitive delays as in the FET.

For most semiconductor NWs in the non-ballistic transport regime, the carrier transit time depends on the electrical field, for instance, Si at E=10kV/cm, the electron velocity is around $7\text{x}10^6$cm/s,[9] and the carrier transit time (t_{LET}) can be estimated to be 7.1ps for a 500nm long Si NW. Considering a switching time (t_{LET})=7.1ps, an on-current of I_{sd}=1μA under V_{sd}=1V, the electrical switching energy E_{el} *(=* I_{sd} *x* V_{sd} *x* t_{LET}*)* will be of the order 7.1aJ/switch. However, in the LET, optical gating power ($P_g = E_{ph}I_{sd}/(eG)$, where E_{ph}

is the photon energy, G is the photo-conductive gain) also contributes to the total switching energy.[4] Assuming E_{ph}=2.5eV, G=10^3, to have I_{sd}=1μA, we get P_g=2.5nW. Then, considering t_{LET}=7.1ps, the optical switching energy E_{op} will be 1.8x10^{-2}aJ/switch << E_{el}, which leaves sufficient room allowing for below100% light power delivery efficiency. A large prototype LET device made of CdSe NW yielded I_{ds}=0.35μA at V_d =1.43V when illuminated with 110nW at 532nm, and an estimated total switching energy ($E_{tot,sw}$ = E_{el} + E_{op}) of 0.06fJ/switch,[4] which is almost an order of magnitude better than typical FETs. Moreover, because of a very low dark current (I_{ds}~1pA), the I_{on}/I_{off} ratio for a LET could be as high as 10^6,[4] which is almost an order of magnitude better than that of advanced FETs, which can reduce the leakage in the access paths of a hybrid SRAM.

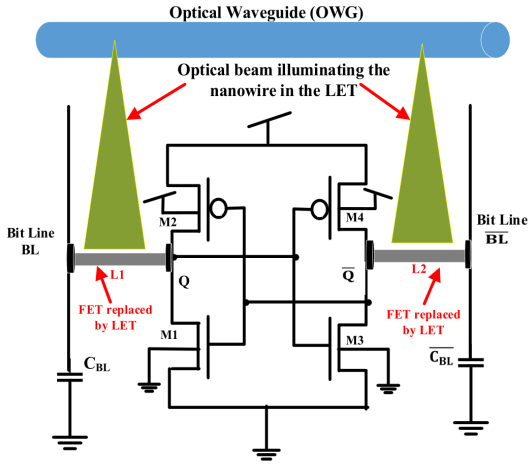

Fig. 2: A prototype hybrid 6T SRAM cell

In a hybrid 6T SRAM, the two access FETs of a regular 6T SRAM are replaced by two LETs (L1 and L2) as shown in Fig. 2. To quantify the potential improvements, a LET with generic semiconductor NW of L=500nm (length) and D=70nm (diameter) and a drive current of 25μA is considered. Numerical analyses show that by replacing the FET access devices by LETs in hybrid arrays of size 256 bytes–512KB give an average improvement of 24 and 21 respectively on read delay and read energy, and an average improvement of 3 and 5 respectively on write delay and write energy.

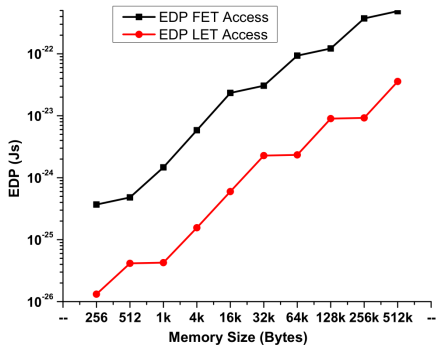

Fig. 3: EDPs of regular and hybrid SRAM arrays

The figure of merit (FOM) or performance evaluation of a SRAM array can be found from the energy-delay product (EDP).[10] Considering a 50% probability of the SRAM array being accessed and for each of the read and write operation,[10] it can be shown that the hybrid SRAM arrays on an average exhibit almost two orders in magnitude smaller EDP than the regular 6T SRAM arrays as shown in Fig. 3.

Also, hybrid SRAMs with a smaller drive current and dimension for the LET access devices (with drive current of 5μA and L=300nm and D=50nm) are considered. It is found that for the same range of the array sizes, the average improvements over regular 6T SRAM structures are 5 and 24 respectively on the read delay and read energy, and 3 and 5 respectively on write delay and write energy

It is evident that for the case of higher drive current (5 times) and device dimension of the access LETs in the hybrid 6T array, the average ready delay improvement is more drastic, while the average write delay is almost same for the two cases, since for large arrays it predominantly depends on the write circuitry current.[10] The average read and write energies are almost unchanged with slight increase due to the increase of optical gating energy (E_{op}) and electrical switching energy (E_{el}) per LET device. Consequently, the average EDP of the hybrid array with larger drive current and device dimension is slightly larger (< 5%) than the other case. So, it may not be very advantageous to increase the drive current of the access LETs in a hybrid 6T SRAM array since the overall energy consumption increases and figure of merit decreases.

Overall, the hybrid 6T SRAM gives greatly improved performance along with much smaller energy consumption over the regular 6T SRAM, and the proposed hybrid SRAM architecture offers close electronic-photonic integration on the same chip with both electronic and photonic devices playing active roles synergistically.

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