Design of all-optical Chalcogenide T-flip flop using Photonic Crystal Waveguide

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***Abstract*-The field of designing photonic crystal based all optical devices is the recent research trend as it remarkably promises an opportunity to diminish circuit complexity. The main intention of this present work is to contrive novel photonic crystal waveguide based all optical chalcogenide T-flip flop. Finally the efficient performance is numerically demonstrated to show elevated values in terms of contrast ratio and field distribution.**

I. INTRODUCTION

Quite recently, the domain of optical devices remains as the central fascinating research field tending to replace digital computing techniques owing to its matchless merits such as ultra-high speed, greater switching actions and wide bandwidth. Therefore, all-optical devices were found applicable in high speed optical networking and computing. Literature supports plethora of design techniques using several technologies has its own realization challenges and few of those are highlighted. For instance design of all optical devices using optical fiber [1] is non-trivial from chip scale integration, while Interferometers [2] based design encounters issues in terms of complex integration, whereas semiconductor optical amplifiers [3] experiences reduction in speed of operation and noise effect and moreover use of photonic crystal ring resonators [4] necessitates elevated input power. In order to tackle these disadvantages, photonic crystal waveguides [5] based design of all optical devices were used as it offers assorted traits such as low power consumption, smaller in size and robust light confinement. In this regard, our intention is to propose a novel design of photonic crystal waveguide based all-optical chalcogenide T flip flop.

The proposed T-flip flop structure is contrived as two dimensional photonic crystals by means of carefully arranging the chalcogenide glass as the refractive index in an exclusive arrangement of line waveguide in X-Y directions. The finite-difference-time-domain (FDTD) method based numerical investigation is executed to assess the light propagation through the designed waveguide structure.

II. DESIGN ASPECTS

The central notion of T-flip flop design aspect is illustrated in Fig.1 and is ascertained by embedding an array of 26 X 13 chalcogenide rods exposed to air substrate arranged in square lattice maintaining lattice constant a=600nm. The projected design is the concatenation of XOR gate with D-flip flop. The radius of these rods is optimized to have r_h=0.19a and the small rods r_e = 0.1a are positioned at the edge nearby coupling region so as to obtain more contrast ratio in terms of realizing distinctive power level. The coupling length is created in operating region of the D-flip flop by removing few of the rods and its length is tailored to be L_C = 5.8a [5]. The occurrence of multimode interference effect at a resonant wavelength of 1550nm is used to implement T-flip flop.

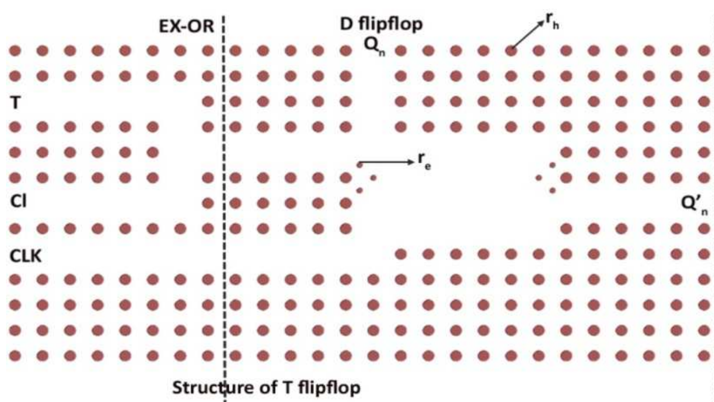


Fig.1. Schematic structure of all optical T-flip flop

A. *Functional operation of T-flip flop*

As illustrated in Fig.2, the entire structure comprises of three input ports namely T, Cl (control input logic) and Clock (Clk) and two output port to be precise Q_n and Q_n' respectively. To verify the toggle logic action, actual input bits in the form of light beam is energized through T input port. Here the input port Cl corresponds to previous state appears at the output of T-flip flop which is represented as Q_n.

T	Cl/Q_n	D	Clk	Q_n	Q'_n
0	0	0	1	Q_n	Q'_n
0	1	1	1	Q_n	Q'_n
1	0	1	1	Q'_n	Q_n
1	1	0	1	Q'_n	Q_n

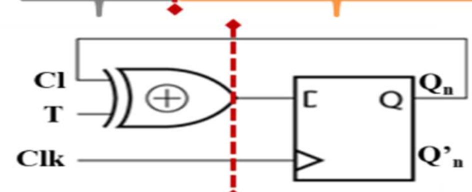
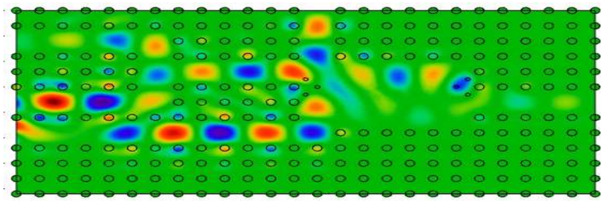


Fig. 2 Truth table with logic diagram for T-flip flop

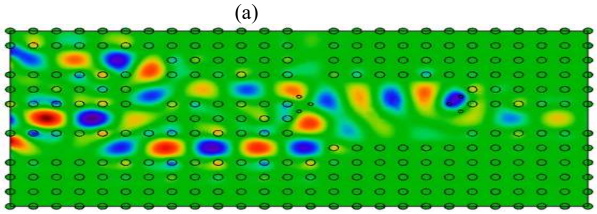
Clk input port is energized with positive level triggering. The XOR logic section accepts the inputs from 'Cl' and 'T' ports to generate 'D' logic values. As illustrated in Fig.2, the D-flip flop section accepts the inputs from 'Clk' port and the output of XOR section is energized as input as given in the above equation Eq.1.

$$D = T \oplus Cl \tag{1}$$

The realization of clocked D-flip flop provides delay or buffer with its input. As illustrated in Fig.3 (a) & (b) (i)When the input port 'T' is energized with no light ray equivalent to 'logic 0', whatever the optical logic state applied in 'Cl' input port gets confined through the waveguide to reach Q_n at the output of X-OR section as 'D' value, meanwhile (ii) when the input port 'T' is assigned with 'logic 1', whatever the optical logic state applied in 'Cl' input port undergo logic inversion to reach at the output of X-OR section as 'D' value.



(a)



(b)

Fig. 3 Field distribution illustrating (a) T=0, Cl =1, Clk =1
(a) T=1, Cl =1, Clk =1

Fig.4 shows the contrast ratio as a means to understand power level difference between optical 'logic 0' and 'logic 1' state. The contrast ratio is measured using the relationship given by

$$CR = 10\log\frac{P_1}{P_0} \tag{2}$$

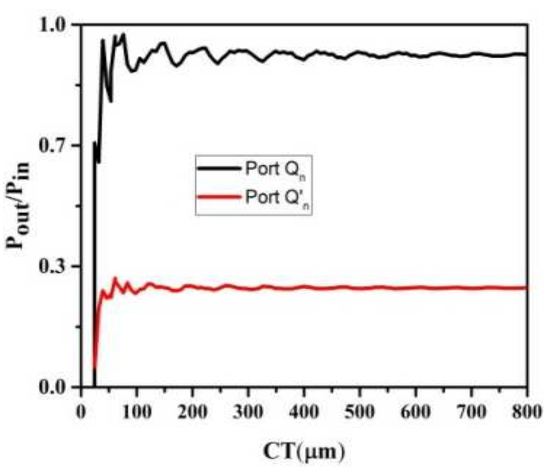


Fig. 4 Power levels measured at Port Qn and Qn'

The distinguishable power level P_0 to vary below 0.28 is used to represent optical logic 0 through Qn port. In the same way, the power level P_1 above 0.89 value denotes optical logic 0 through Qn' port.

III. CONCLUSION

In this work, all optical T-flip flop is realized with photonic crystal waveguide composing of an array of chalcogenide rods in square lattice. The efficacy of this design is mathematically examined utilizing the FDTD technique and the appropriate use of chalcogenide glass material offered high value of contrast ratio to distinguish the optical logic 0 and logic 1. It is apparent that this latest proposed T-flip flop is anticipated to contribute to the development of gadgets and circuit sub-modules for high velocity broadband optical communication and networking frameworks.

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