Balanced Optimization of 1310 nm Tunnel-Junction VCSELs

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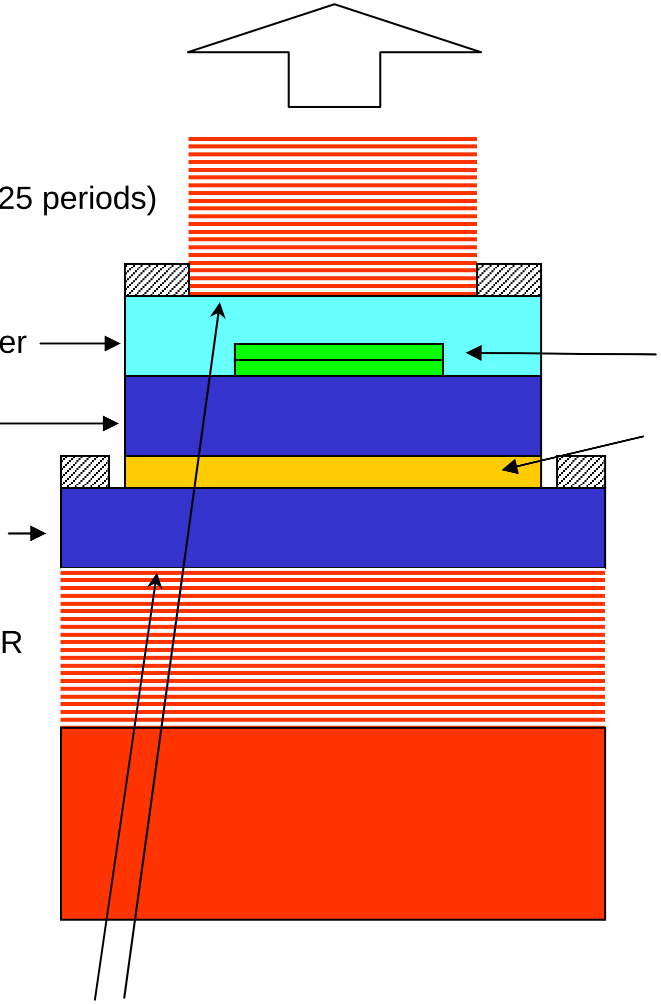
Outline

1. Introduction
2. Experimental Results
3. Numerical Analysis
4. Design Optimization
5. Summary

VCSEL Design



GaAs/AlGaAs DBR (25 periods)

n-InP contact layer →

AlInAs/InP tunnel junction

p-InP →

InGaAlAs MQW

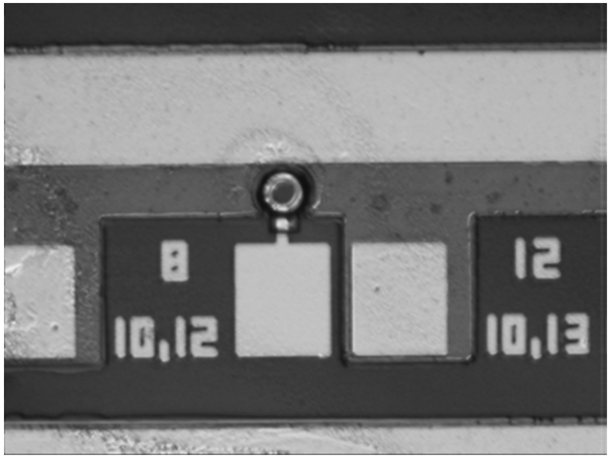
n-InP contact layer →

GaAs/AlGaAs DBR
(31 periods)

GaAs substrate

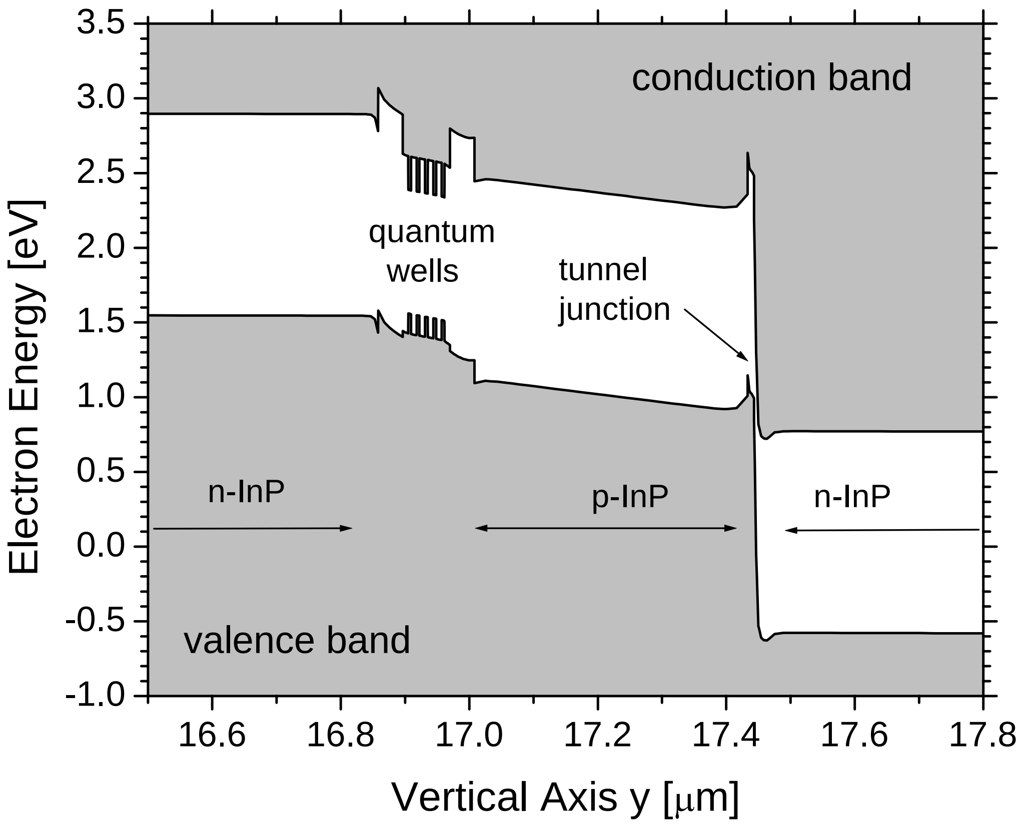
☺ exact definition of aperture

☺ no current flow through bonded interfaces



Active Region with Tunnel Junction

Energy Band Diagram



Advantage

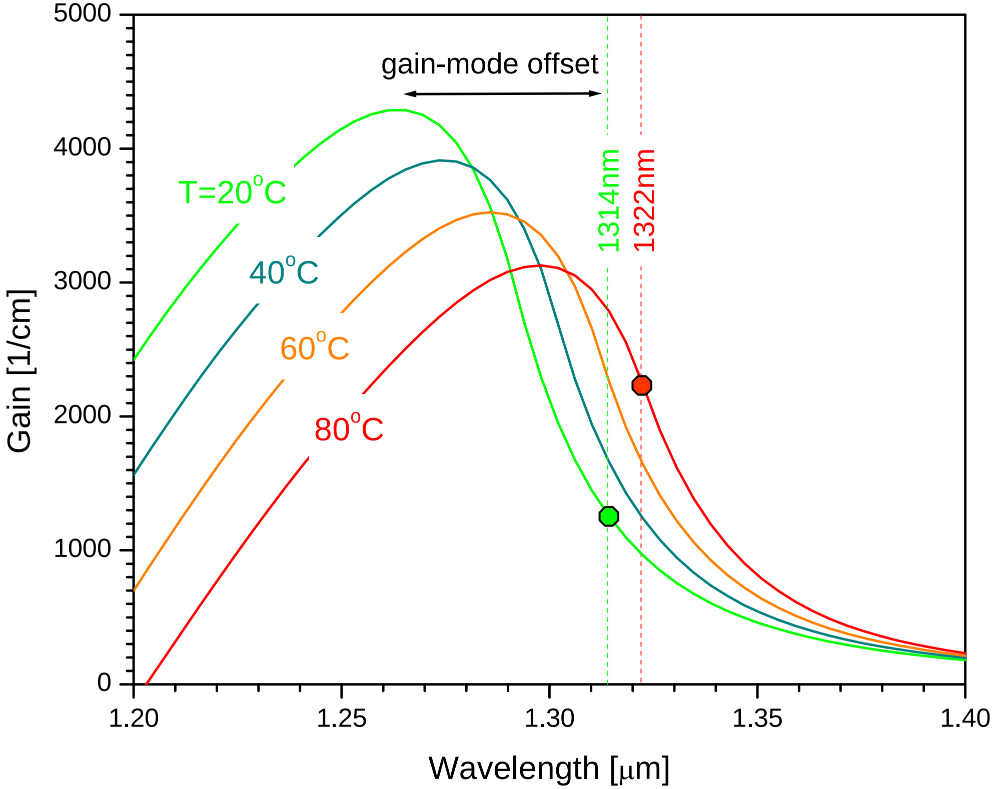
- reduced p-region
- less absorption
- lower resistance
- no p-p bonding

Device Overview

Device	Aperture size	gain-mode offset
A	8 µm	66 nm
B	12 µm	51 nm
C	8 µm	51 nm

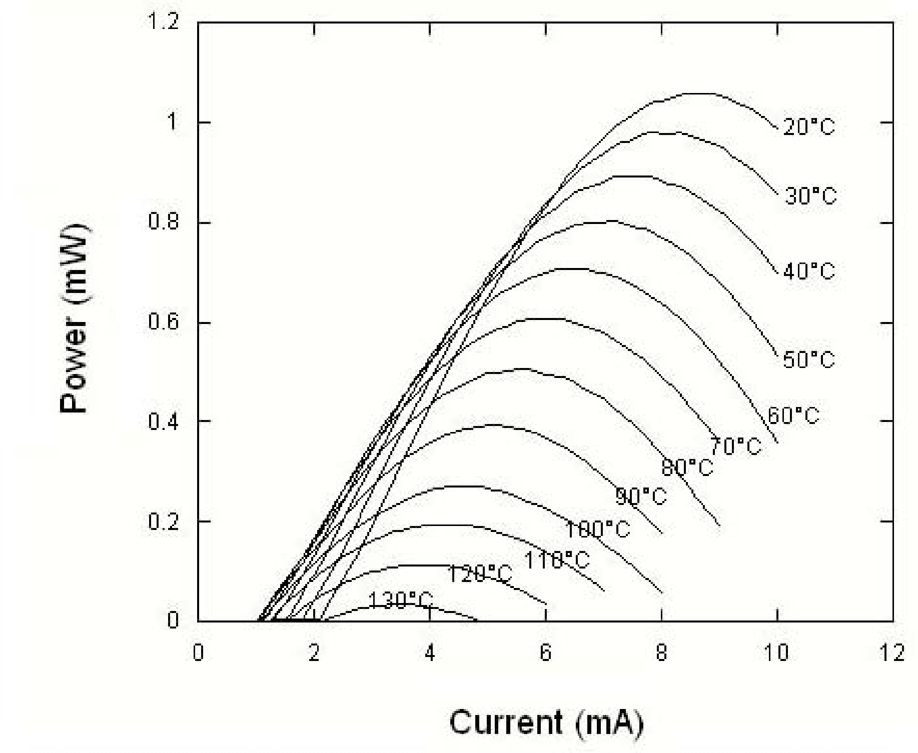
Gain - Mode Offset

larger offset allows for higher lasing temperatures
but less gain / power at room temperature



High-Temperature CW Operation

(A) T_{max}=134^{o}C - highest ever achieved with long-wavelength VCSELs



- 8 µm aperture
- gain-mode offset = 66 nm

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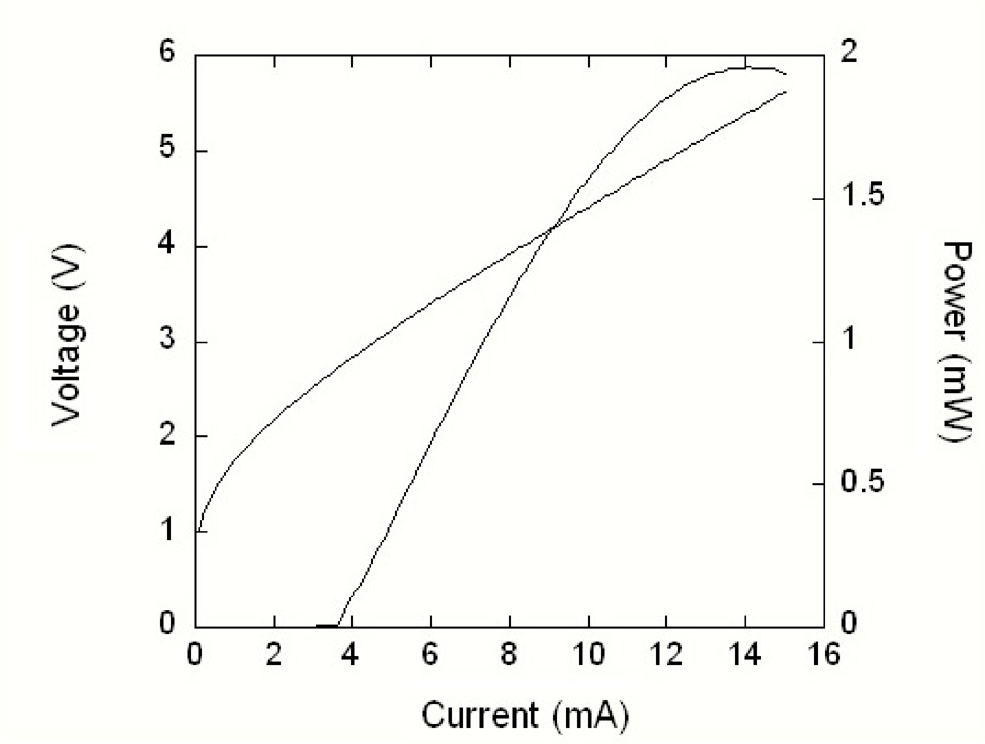
High Power CW Operation

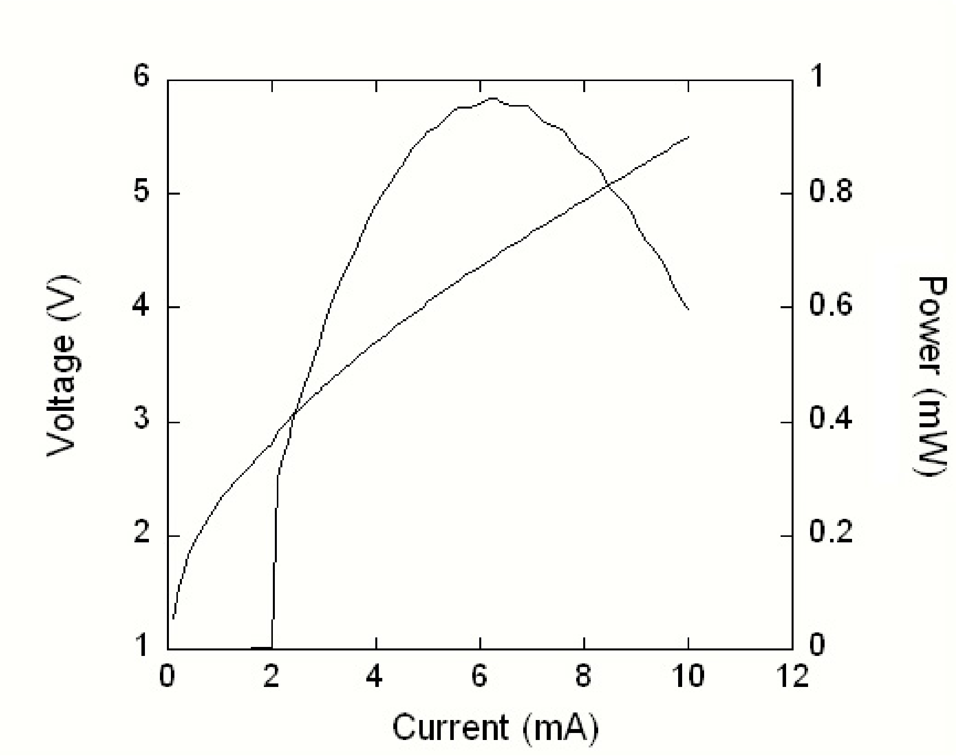
(B) lower offset gives ~2 mW room temperature output power

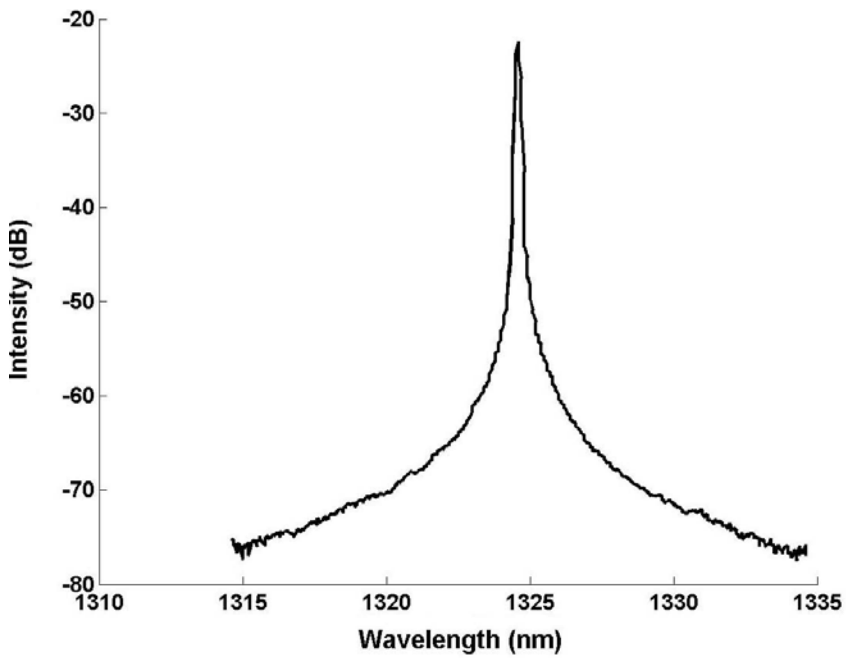


- 12 μm aperture
- Diff. Quantum Eff. = 30%
- gain-mode offset = 51 nm
- Device operation to 100°C

Single Mode Lasing

(C) lower aperture gives ~1 mW single mode output power at 66°C





- 8 µm aperture
- Device operation to 123°C

- gain-mode offset = 51 nm
- > 30dB side-mode suppression

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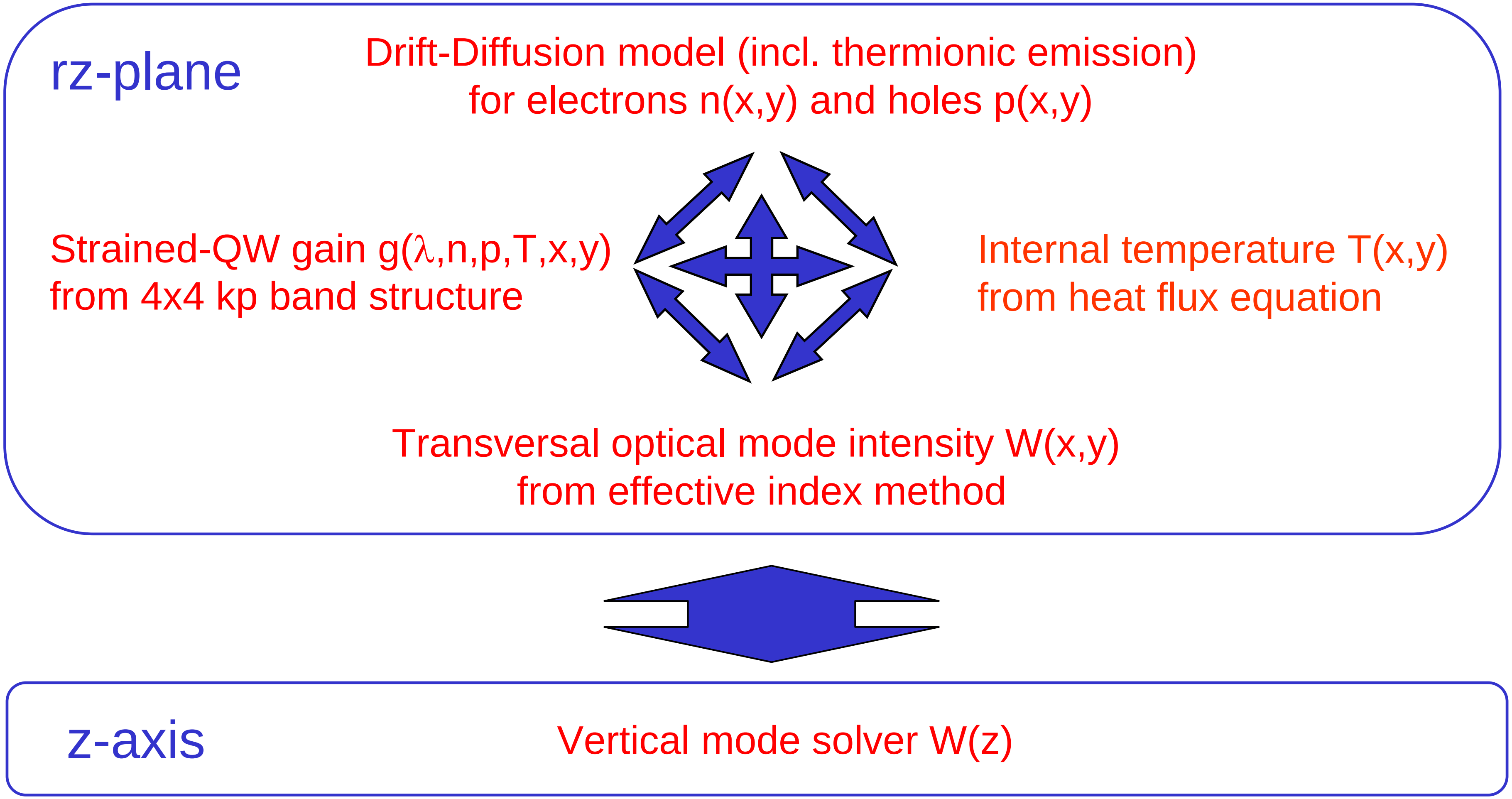
PICS3D: Self-Consistent VCSEL Model



rz-plane

Drift-Diffusion model (incl. thermionic emission)
for electrons n(x,y) and holes p(x,y)

Strained-QW gain g(λ,n,p,T,x,y)
from 4x4 kp band structure

Internal temperature T(x,y)
from heat flux equation

Transversal optical mode intensity W(x,y)
from effective index method

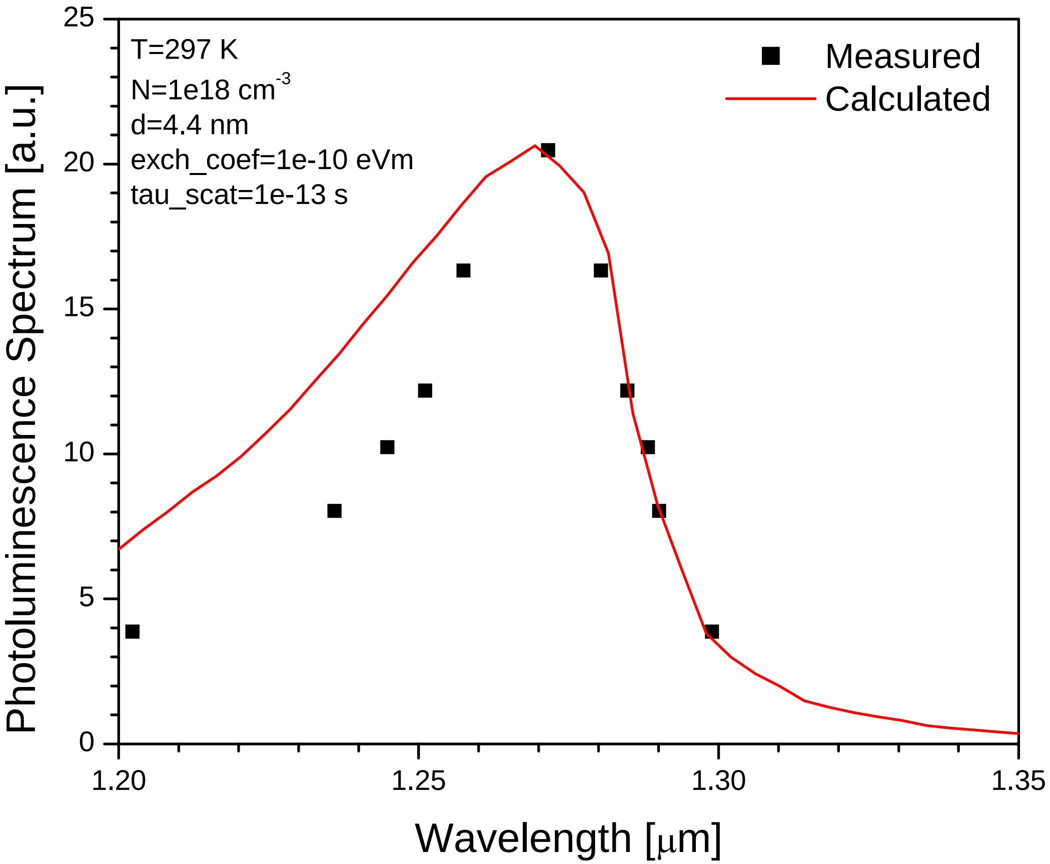
z-axis

Vertical mode solver W(z)

www.crosslight.com

[J. Piprek, *Semiconductor Optoelectronic Devices – Introduction to Physics and Simulation,* Academic Press, San Diego, 2003]

Comparison to measurements: PL



free-carrier model:

photoluminescence (PL) and gain overestimated for short wavelengths

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Parameter Calibration for Threshold Current

Auger recombination rate

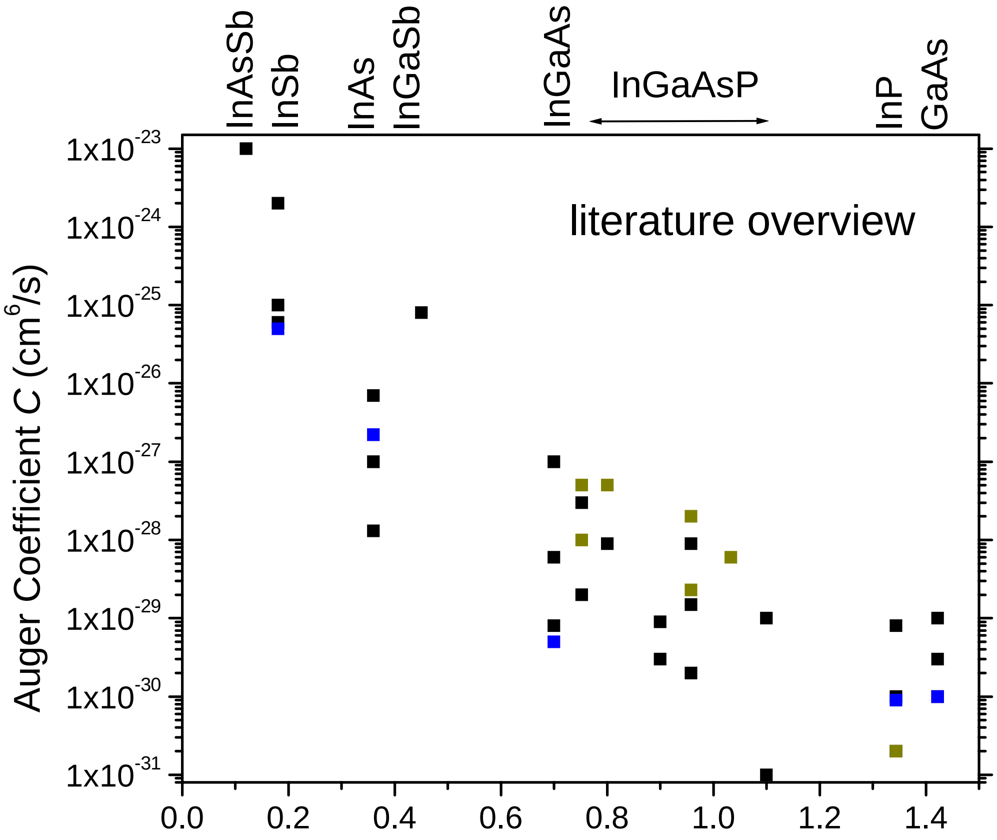
$$R_{Aug} = \left(C_n n + C_p p\right)\left(np - n_i\right)$$

$$C\ (20^o C) = 1.15\times10^{-29} cm^{-6} s^{-1}$$

$$C\ (T) = C_0 \exp\left[-\frac{160meV}{kT}\right]$$

Defect recombination lifetime

MQW $\tau_{SRH} = 10\ ns$
elsewhere $\tau_{SRH} = 100\ ns$



Parameter Calibration for Slope Efficiency

Intervalenceband and free carrier absorption

$\alpha_{fc} = k_p\, p + k_n\, n$ $k_p = 13 \times 10^{-18} \mathrm{cm}^2$

$k_n = 2 \times 10^{-18} \mathrm{cm}^2$

Background absorption (fit) $\alpha_b = 3$ /cm

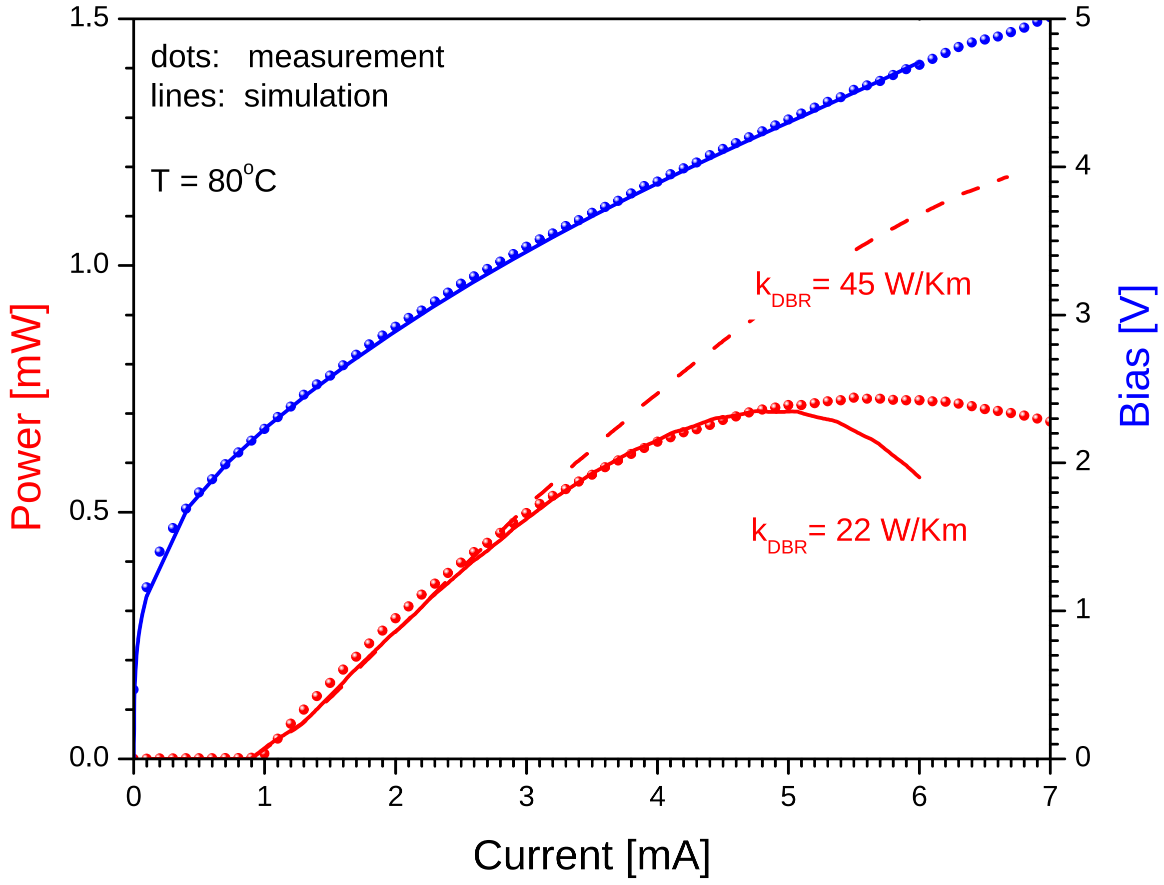
Band offset $\Delta E_c / \Delta E_g = 0.72$ for AlGaInAs

$\Delta E_c = 292$ meV, $\Delta E_v = 147$ meV for InP/AlInAs

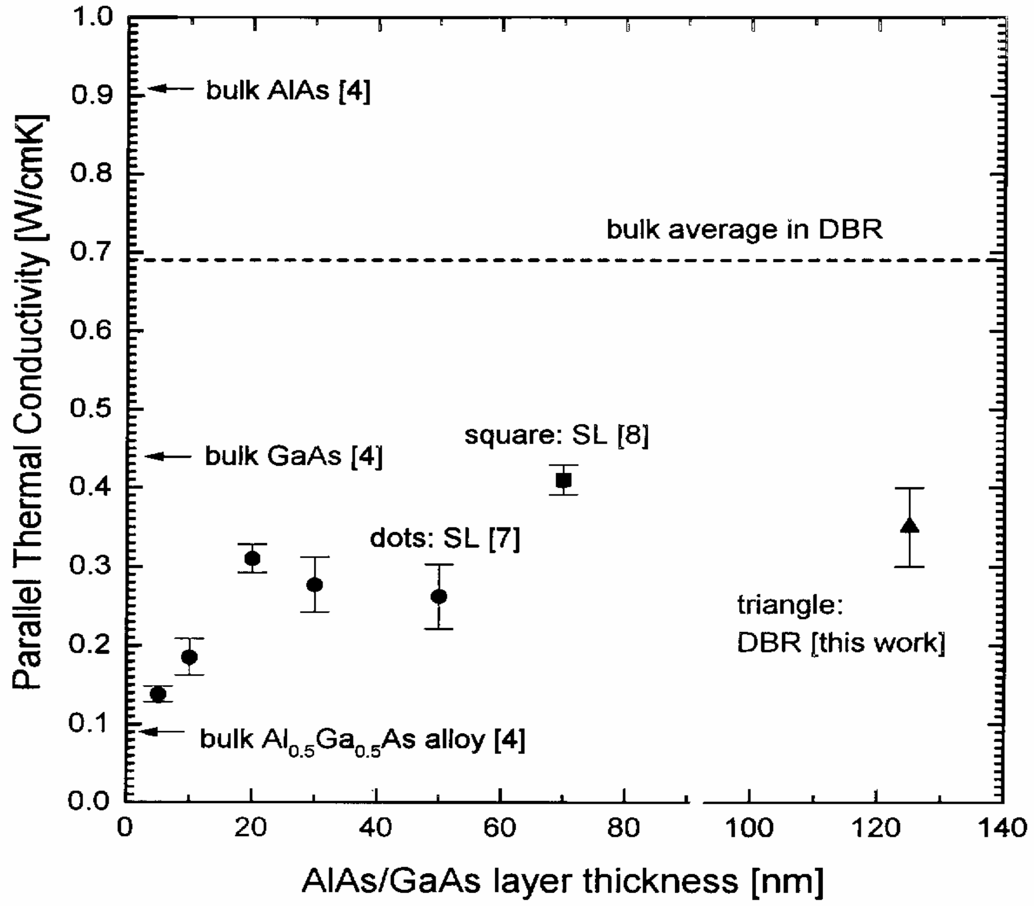
Band shift $dE_g/dT = 334$ meV/K as measured

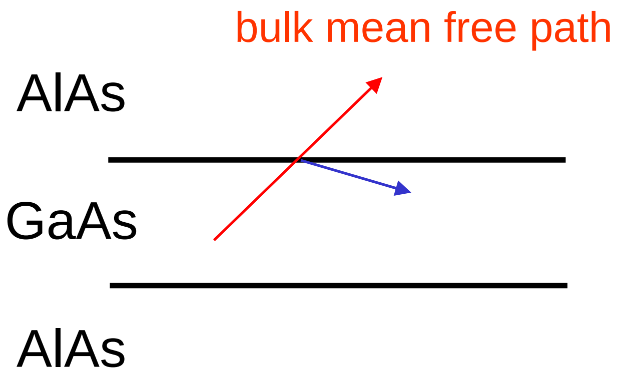
Comparison to Measurement: LIV

fit parameter: DBR thermal conductivity k_{DBR}



AlAs/GaAs DBR Thermal Conductivity Limitation





bulk mean free path

AlAs

GaAs

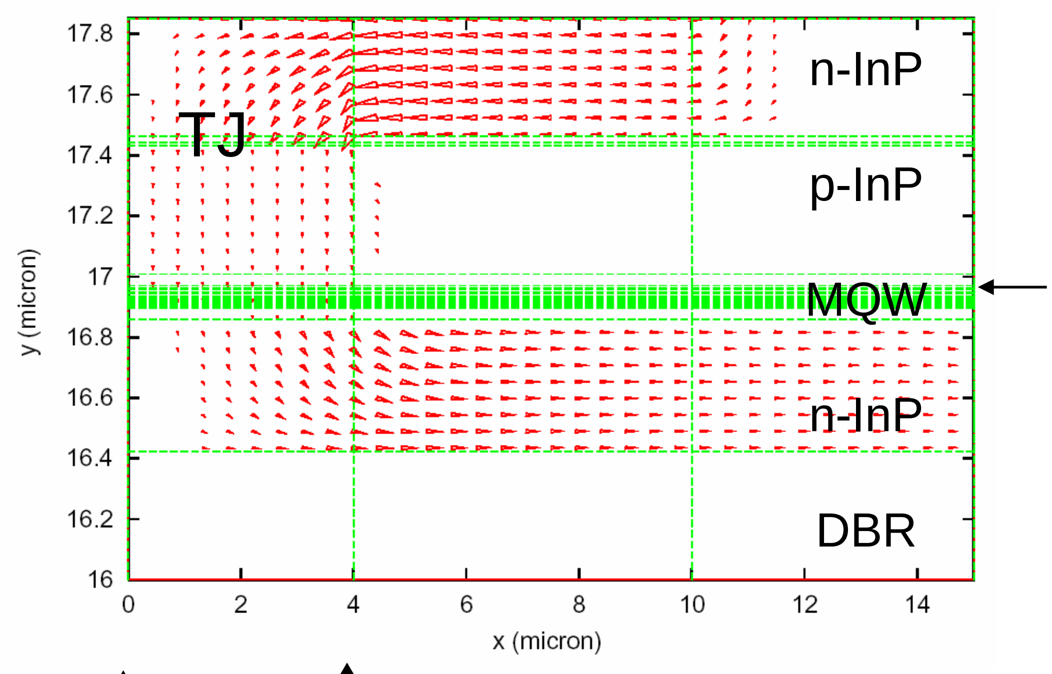
AlAs

DBR interfaces restrict phonon mean free path

[J. Piprek et al., IEEE Photonic Technology Letters, Vol. 10, No. 1, pp.81-83 (1998)]

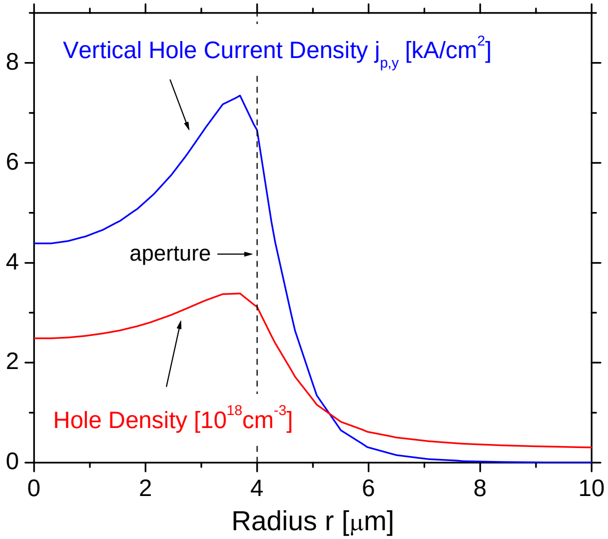
Analysis: Carrier Confinement

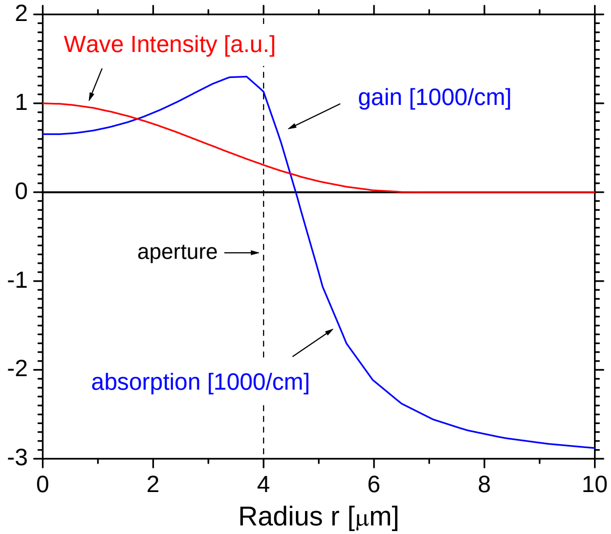
current flow



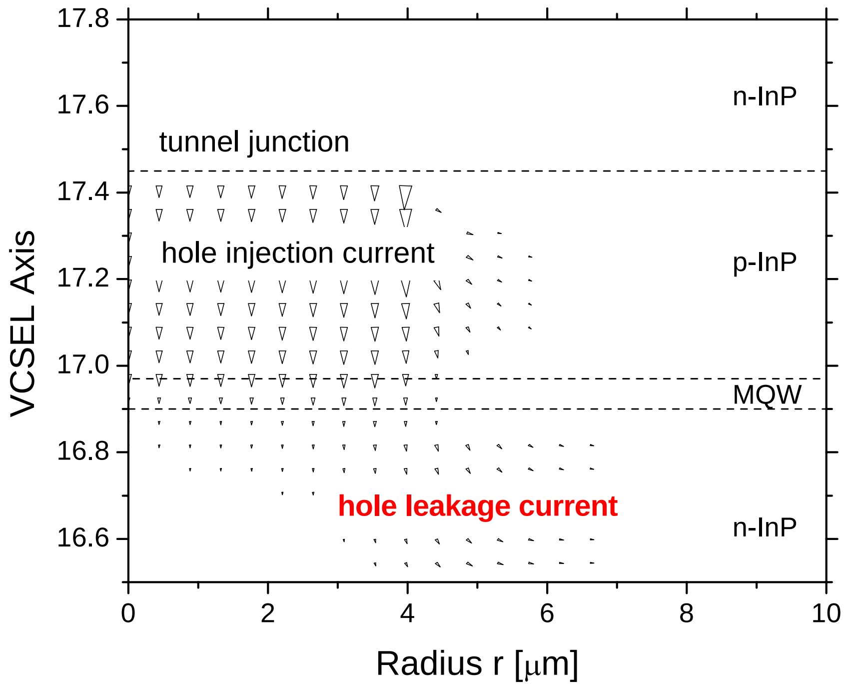
tunnel junction (TJ) aperture

VCSEL axis

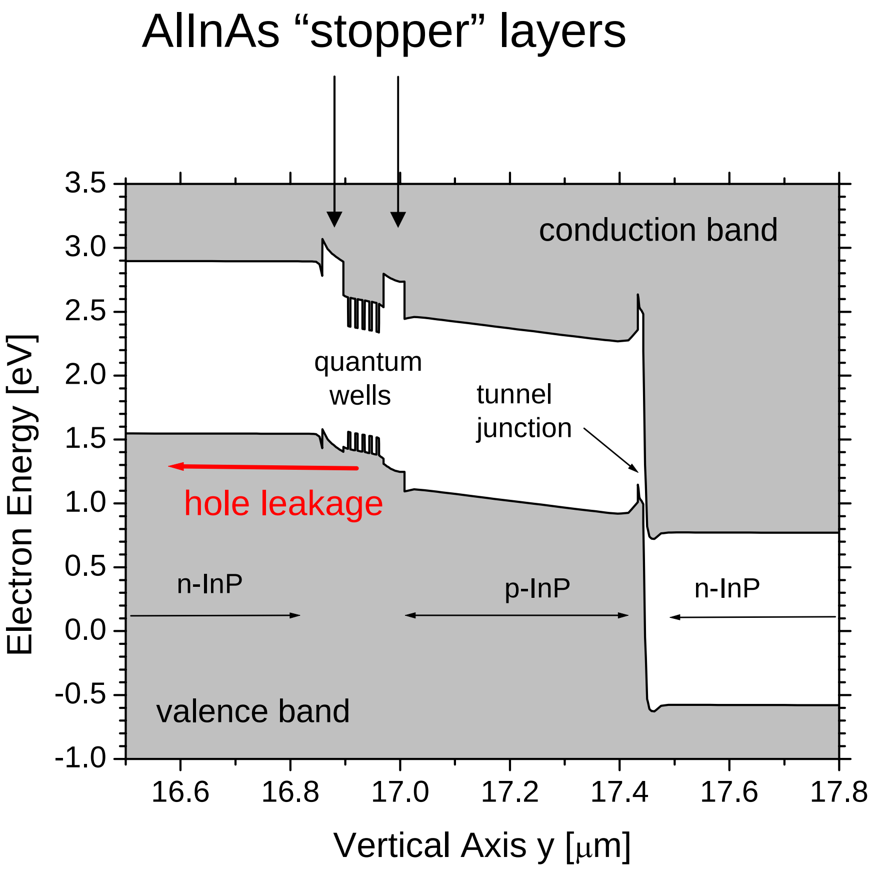




Analysis: Hole Leakage



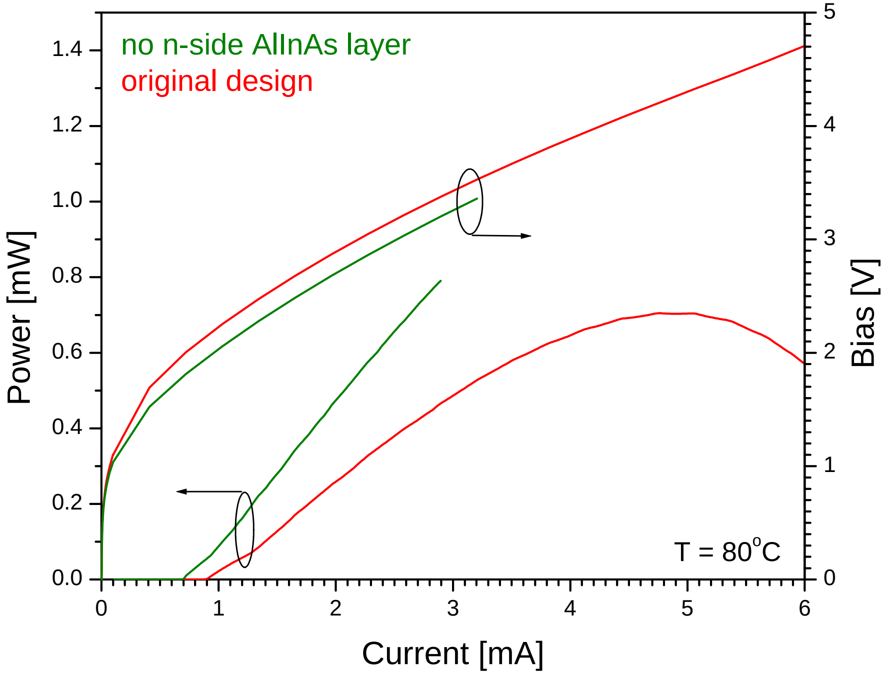
AlInAs “stopper” layers

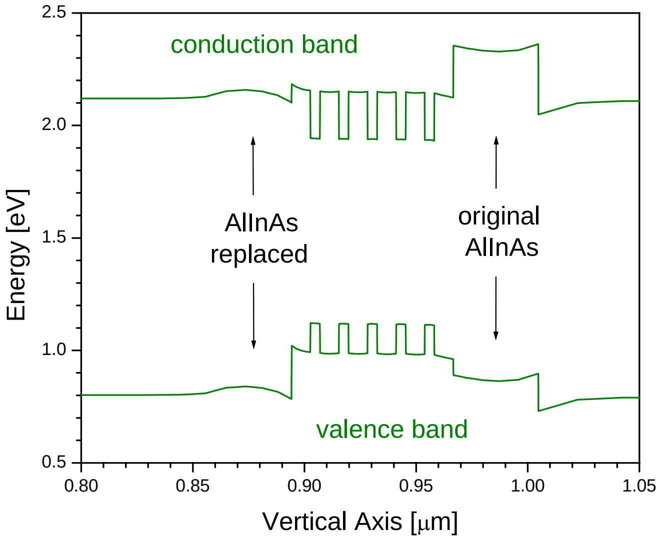


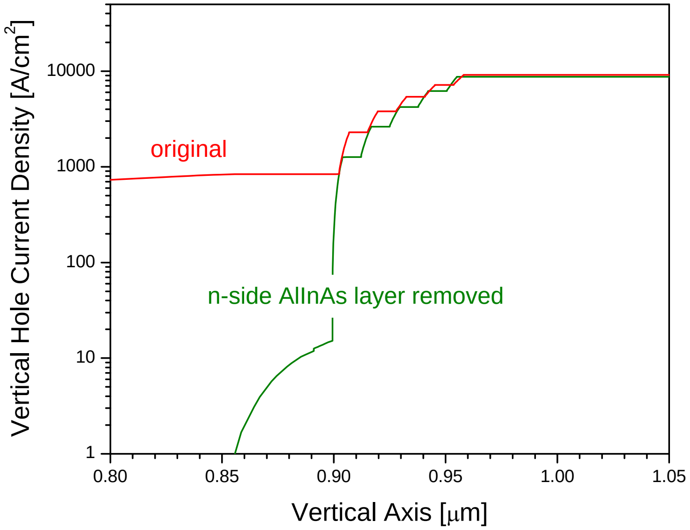
Optimization Targets

1. Reduce leakage, enhance slope efficiency
2. Reduce bias, limit self-heating
3. 1 mW single mode power at 80^{o}C

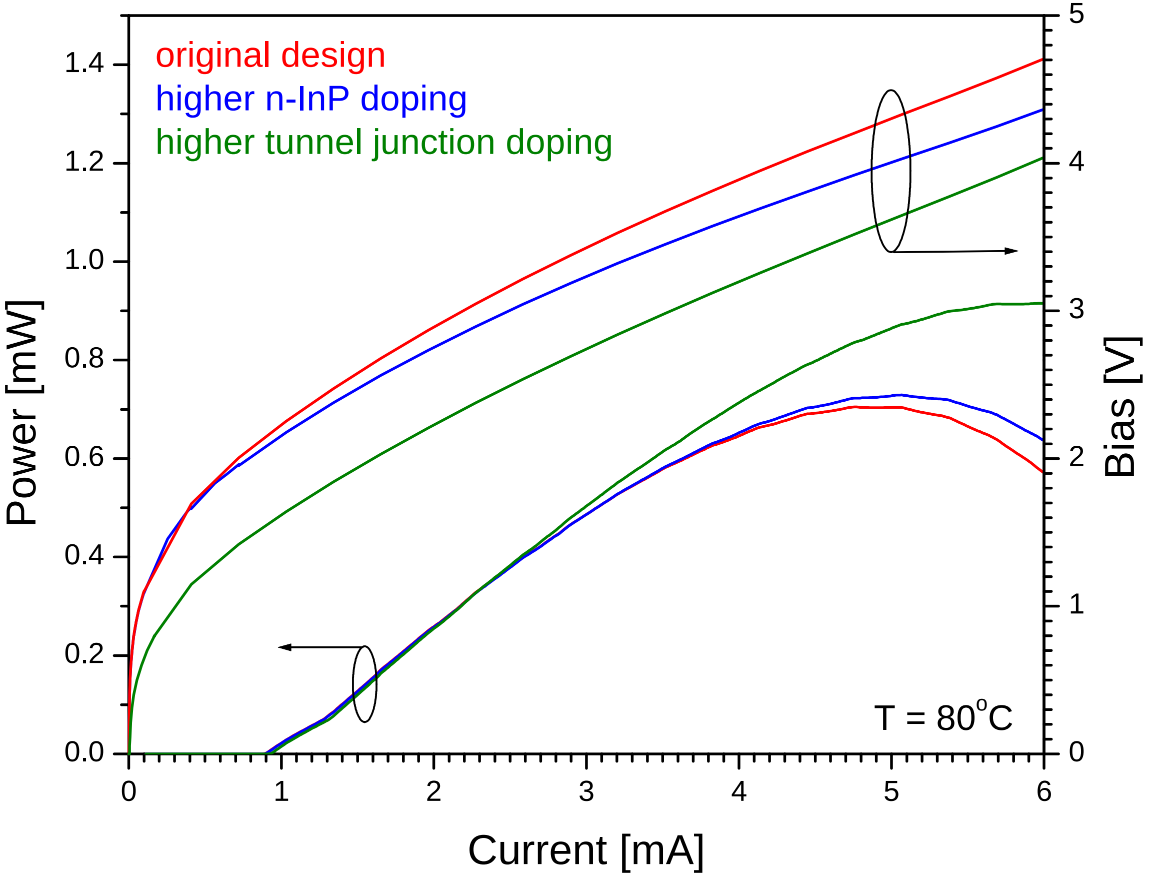
Optimization: Remove n-side AlInAs Layer





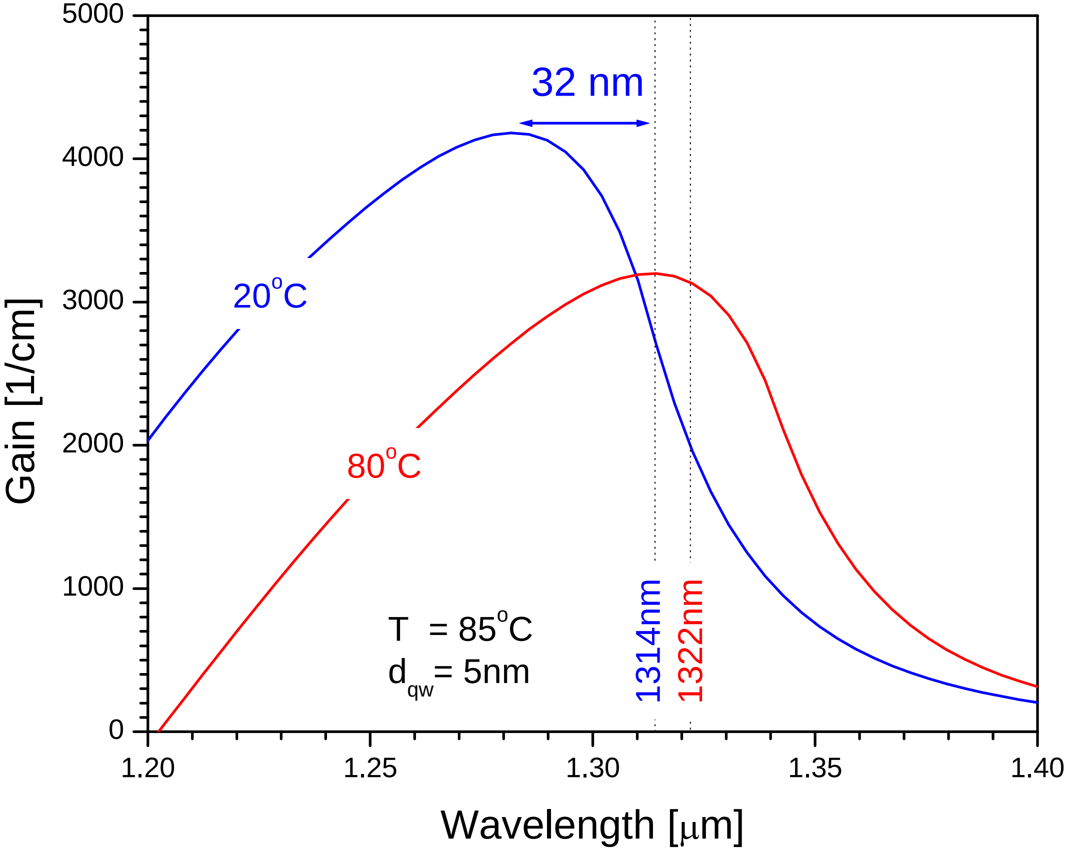


Optimization: Higher n-Doping



Optimization: Gain – Mode Offset

Optimum offset for maximum power = 32 nm (original: 51 nm)



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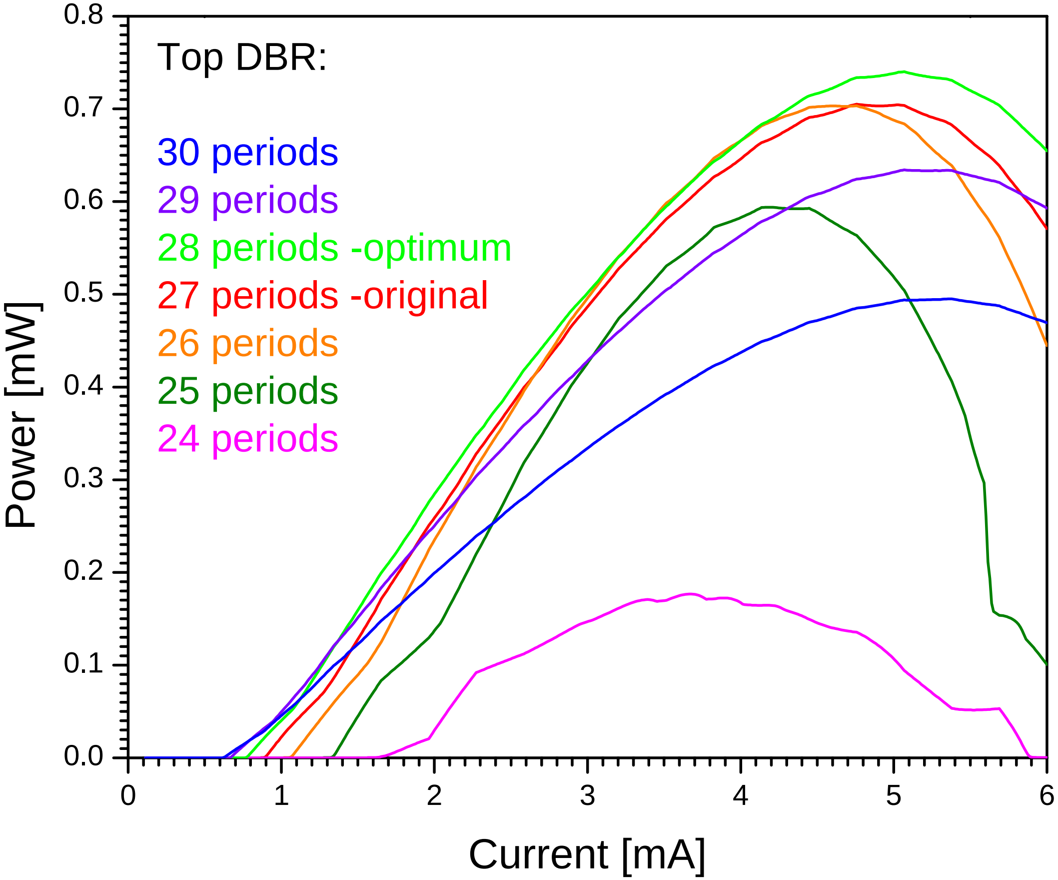
Optimization: Top DBR Reflectivity

Optimum number of top DBR periods = 28 (original: 27)



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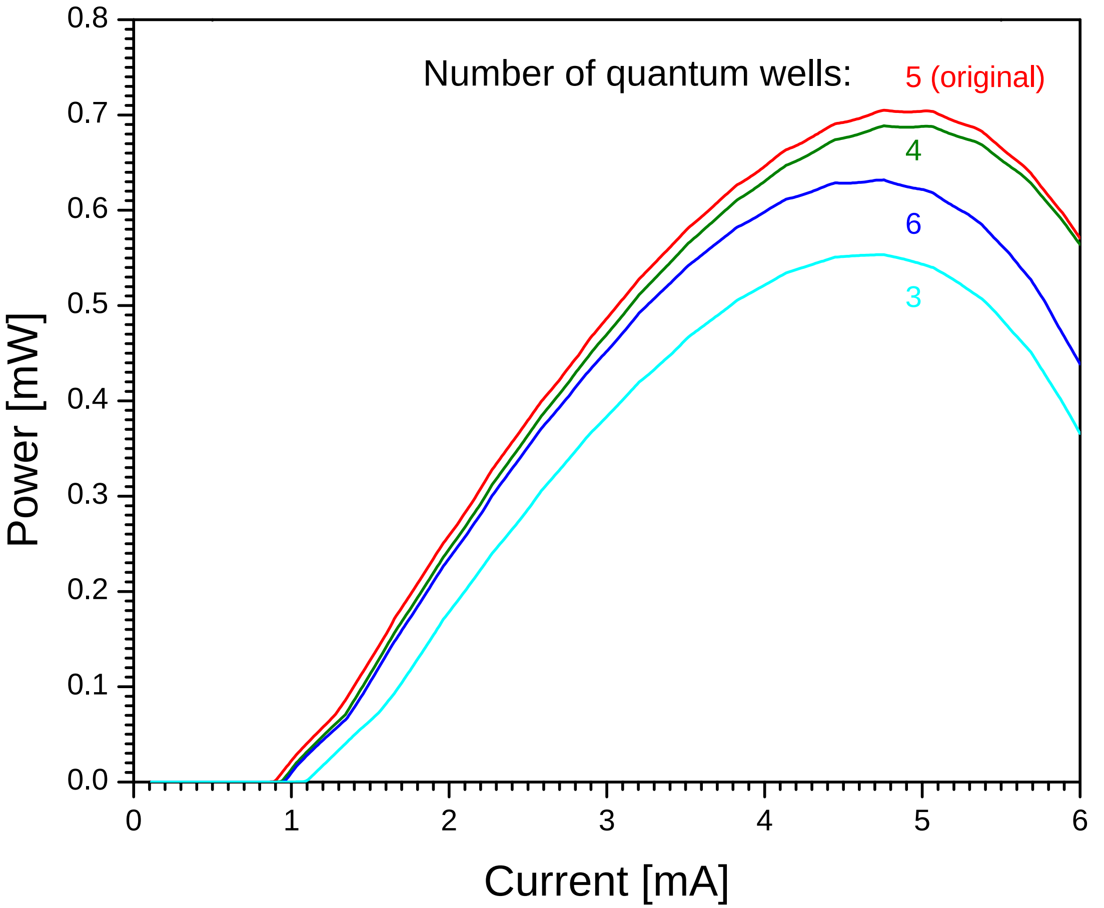
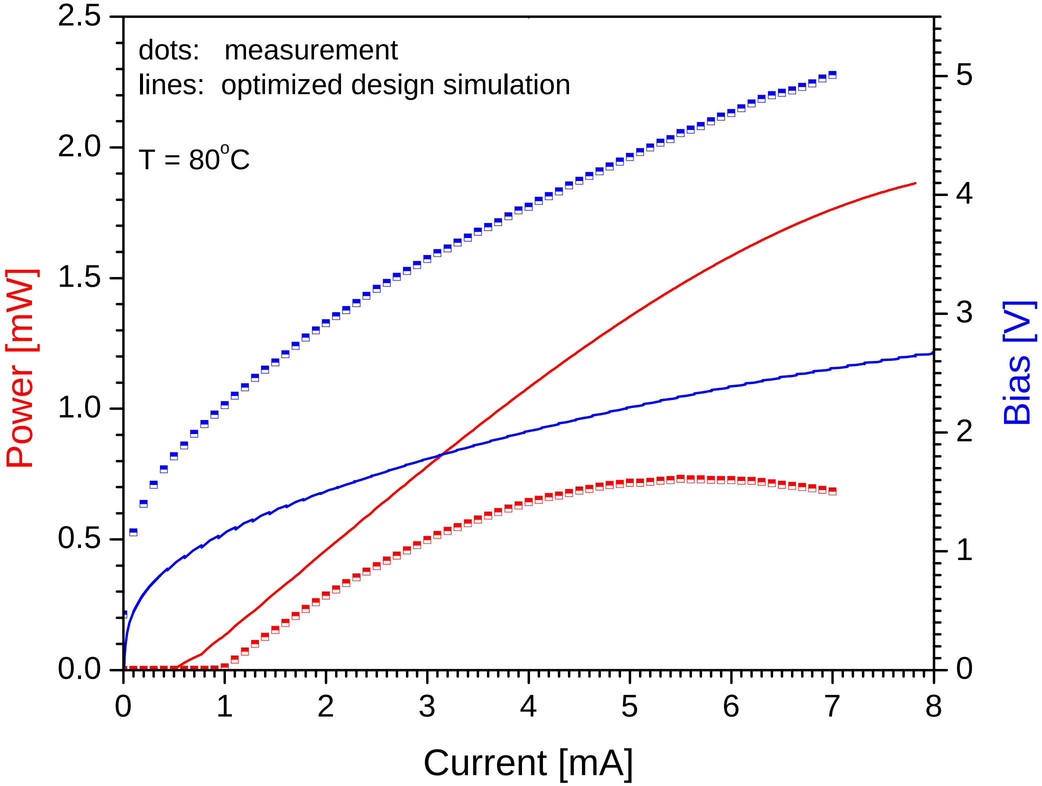
Optimization: Number of Quantum Wells

Optimum number of quantum wells = 5 (original)



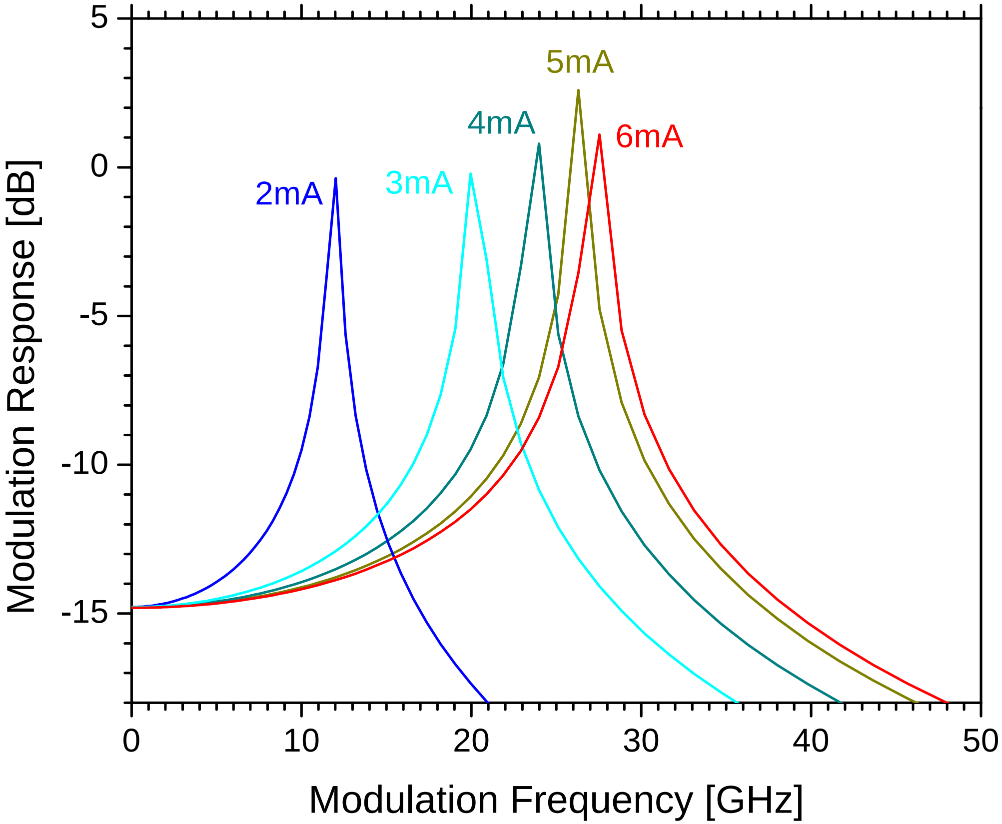
Overall Design Optimization

- remove n-AlInAs layer
- gain offset 51 => 32 nm
- tunnel-junction doping x 2
- tunnel-junction aperture 8 =>10µm
- n-InP regrowth doping x 4
- top DBR periods: 27 => 28



High-Speed Performance

Intrinsic modulation response for optimized design



Summary

balanced design optimization enables

- high temperature (80°C)
- high power (> 1 mW)
- high-speed (f_r > 20 GHz)
- single fundamental mode lasing

- using self-consistent numerical model
- including careful parameter calibration
- agreement with original device measurements

Future: include many-body gain