Thermionic emission cooling in single barrier heterostructures

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Nonisothermal transport in InGaAsP-based heterostructure integrated thermionic coolers is investigated experimentally. Cooling on the order of a degree over 1 μm thick barriers has been observed. This method can be used to enhance thermoelectric properties of semiconductors beyond what can be achieved with the conventional Peltier effect. © *1999 American Institute of Physics.* [S0003-6951(99)02701-1]

Temperature stabilization of optoelectronic components (lasers, filters, switches, etc.) is of increasing importance in many high-speed and wavelength division multiplexed fiber-optics communication systems. Heat generation and thermal management in very large scale integrated (VLSI) circuits is becoming one of the barriers to further increase clock speeds and decrease feature sizes. Solid-state coolers integrated with devices are an attractive way to solve some of these problems. This means alternatives to thermoelectric cooling using Bi_2Te_3, the current industry standard, must be found. A solution is to use thermionic emission in heterostructures, a technique that can give significant cooling in conventional materials such as AlGaAs, InGaAsP, or SiGe.[1,2] In this letter, we investigate experimentally nonisothermal electron transport in InGaAsP-based heterostructure integrated thermionic (HIT) coolers.

The conventional thermoelectric effect is based on bulk properties of materials.[3] When electrons flow from a material in which they have an average transport energy smaller than the Fermi energy to another material in which their average transport energy is higher, they absorb thermal energy from the lattice and this will cool down the junction between two materials. In an alternative method, thermionic emission current in heterostructures can be used to achieve evaporative cooling by selective emission of hot electrons over a barrier layer from cathode to anode.[1,2,4,5] Since the energy distribution of emitted electrons is almost exclusively on one side of the Fermi energy, upon the current flow, strong carrier–carrier and carrier–lattice scatterings tend to restore the quasiequilibrium Fermi distribution in the cathode by absorbing energy from the lattice, and thus, cooling the emitter junction.

In order to investigate experimentally thermionic emission cooling in heterostructures, a single InGaAsP ($\lambda_{gap} = 1.3$ μm) barrier surrounded by n^+-InGaAs cathode and anode layers was grown using metal organic chemical vapor deposition (MOCVD). Cathode and anode layer thicknesses were 0.3 and 0.5 μm and they were doped to 3×10^{18} cm^{-3}. The barrier layer had an n doping of 2×10^{17} cm^{-3} and was 1 μm thick. Mesas with an area of 90×180 μm^2 were etched down using dry etching techniques. Ni/AuGe/Ni/Au was used for top and bottom contact metallization. Figure 1 displays the measured temperature on the top and on the bottom of the device as well as the substrate temperature far away from the device as a function of current. All temperatures are relative to the value at zero current. The rise in substrate temperature is an indication of the relatively high thermal resistance of the ceramic package and the soldering layer used to mount the sample. Despite the poor performance of the heat sink on the anode side, a net cooling of 0.5 °C is observed on top of the device. This cooling over a 1 μm barrier corresponds to cooling capacities on the order of 200–300 W/cm^2. To understand these results a two-dimensional finite difference heat equation solver (ANSYS) was used to simulate the performance of the device. Joule heating in the layers, substrate, and gold wire bonds were included as well as thermionic emission cooling (heating) at the cathode (anode) junction and the thermoelectric (TE) effect at the metal/semiconductor junctions. The position dependence of the Peltier effect and thermionic emission (TI) cooling requires a detailed understanding of

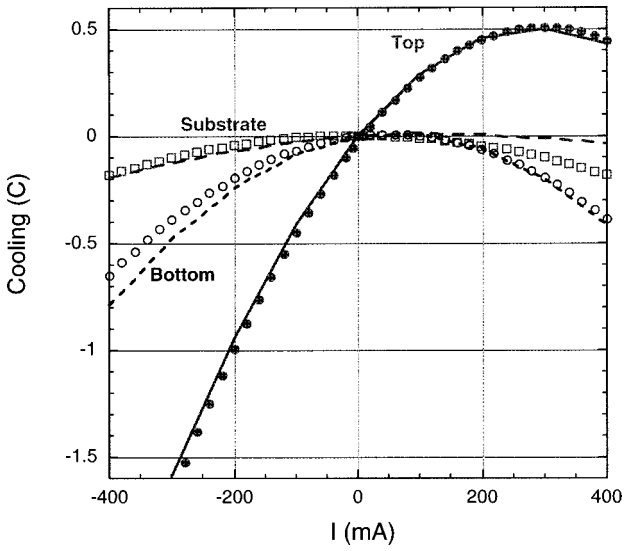

FIG. 1. Measured temperature on the top and on the bottom of the HIT cooler, as well as the substrate temperature far away from the device as a function of current. All temperatures are relative to the value at zero current. The heat sink temperature is 20 °C. The simulation results are the solid curve for the top temperature, short-dashed curve for the bottom temperature, and dashed curve for the substrate.

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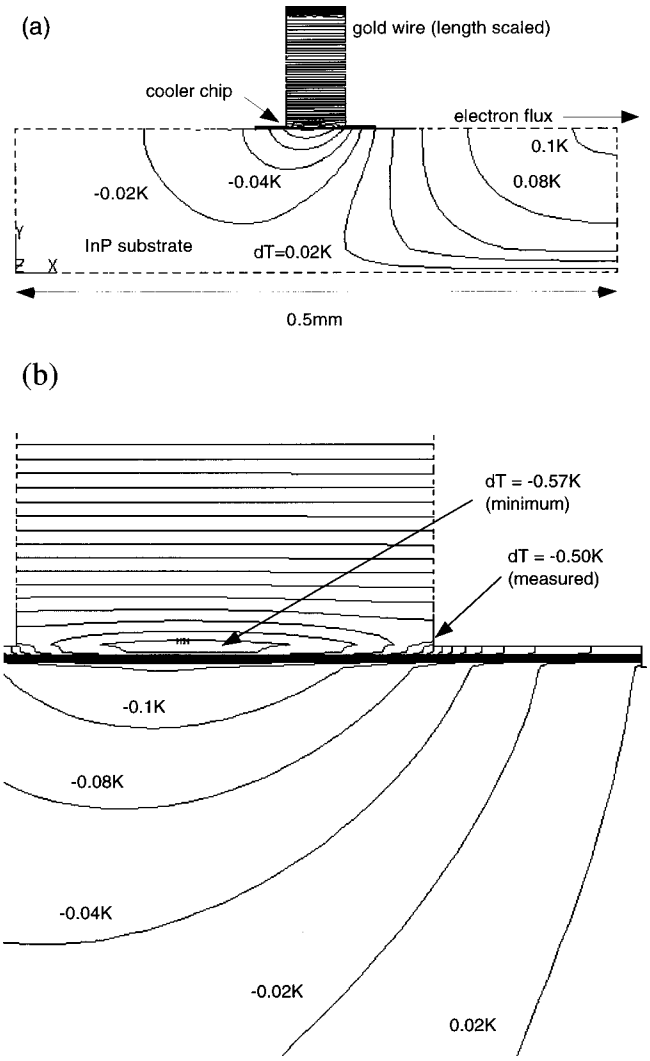

FIG. 2. Contour plot of the temperature profile in the cross section of the device at a current of 200 mA. The whole simulation area shown in (a) and (b) is a magnification of temperature distribution near the device. One can see Joule heating in the wirebonds connected to the device, as well as the poor behavior of the heat sink connected to the hot side of the HIT cooler.

the electron's energy relaxation length for materials and dopings under study.[2] As a first approximation, TE and TI effects were assumed to be heating or cooling sources at appropriate interfaces. The Peltier effect at the junction InGaAs(n^+)/Au was studied by applying current between the two bottom contacts. A cooling 2–3 times smaller than the thermionic cooling was measured.

Figure 2 shows the two-dimensional temperature profile in the cross section of the device. The whole simulation area is shown in Fig. 2(a) and it includes the HIT cooler, 100 μm thick substrate, and gold wirebond to the top contact (its length is scaled in order to reduce the computation time). The wirebond for the bottom contact is 500 μm away from the device and it is not directly included in the calculations. Figure 2(b) displays a magnification of the temperature distribution near the device. One can see that Joule heating in the wirebond connected to the cathode, and heat conduction from the package to the cold junction through this wire is one of the major factors that limits the maximum cooling of the device. Assuming the thermal conductivity of InGaAsP to be 2 W/mK (i.e., 50% of textbook value[6]) and a solder

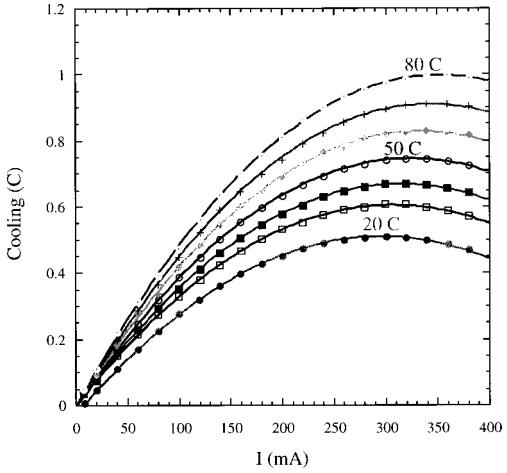

FIG. 3. Measured cooling at various substrate (heat sink) temperatures.

layer and package with total thermal resistance of 2.5×10^3 K/W, the overall cooling and the temperature distribution in the device fit reasonably well the measured values in Fig. 1. In order to minimize the effects of series and contact resistances, a number of *p*- and *n*-type HIT coolers connected electrically in series and thermally in parallel should be used (similar to conventional thermoelectric cooling modules). By improving the packaging, 10 °C cooling for single stage InGaAsP HIT coolers is expected.[2]

Figure 3 displays the measured cooling at various substrate temperatures. The device cools much better at higher temperatures. A net cooling of about 1 °C is measured at 80 °C. The reason for the improved performance is twofold. First, the thermal conductivity of the barrier decreases at higher temperatures, and second, thermionic emission cooling increases due to the larger thermal spread of carriers near the Fermi energy.

In conclusion, thermionic emission cooling in single barrier InGaAsP-based heterostructures is investigated experimentally. Cooling by 0.5° and 1° over a 1 μm thick barrier is reported at 20 and 80 °C, respectively. Simulations show that performance of the device is limited by the wire connected to the cold junction and poor performance of the heat sink at the anode side. With improvements in packaging, 10 °C cooling for single stage InGaAsP HIT coolers is expected. This method can be used with other compound semiconductors (AlGaAs, HgCdTe, SiGe, InGaSb, etc.) and make coolers integrated with electronic components. Theoretical calculations show that single stage cooling by 10°–40° should be possible.[1,2]

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[1] A. Shakouri and J. E. Bowers, Appl. Phys. Lett. **71**, 1234 (1997).
[2] A. Shakouri, E. Y. Lee, D. L. Smith, V. Narayanamurti, and J. E. Bowers, Microscale Thermophysical Engineering **2**, 37 (1998).
[3] H. J. Goldsmit, *Electronic Refrigeration* (Pion, London, 1986).
[4] G. D. Mahan and L. M. Woods, Phys. Rev. Lett. **80**, 4016 (1998).
[5] G. D. Mahan, J. O. Sofo, and M. Bartkowiak, J. Appl. Phys. **83**, 4683 (1998).
[6] S. Adachi, *Properties of InP* (INSPEC, UK, 1993).